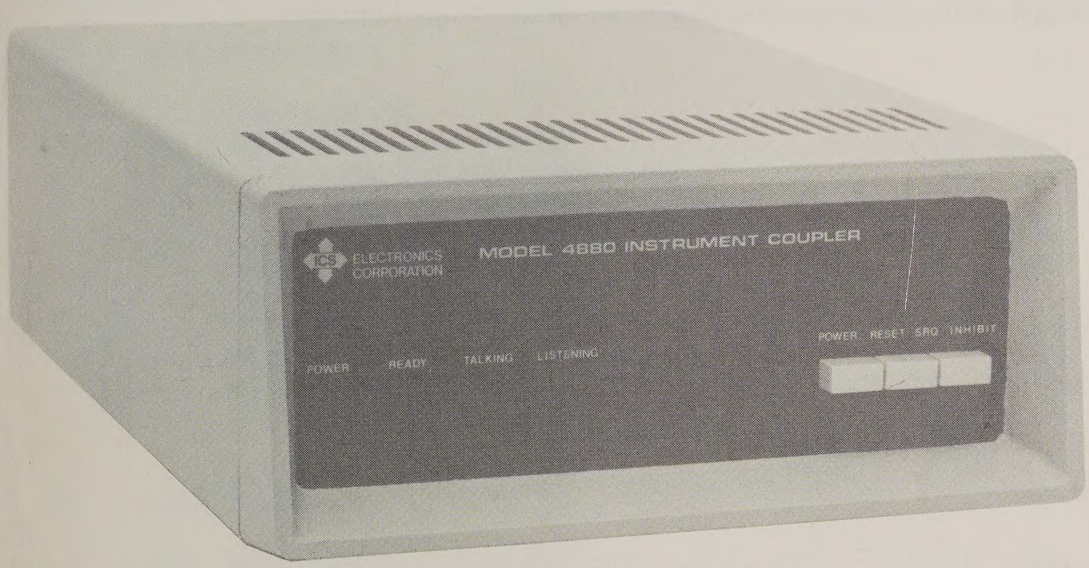
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ICS ELECTRONICS CORPORATION

MODEL 4880
Instrument Coupler Instruction Manual



MODEL 4880
Instrument Coupler Instruction Manual



FOR USE IN THE CALIBRATION OF
COMPANY INSTRUMENTS.
9
QC FACILITIES
DATE: 23. 1. 84.
BRITISH AIRCRAFT CORPORATION, STEVENAGE

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P/N 120003
Revision 5 January 1981

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LIMITED WARRANTY

Within 12 months of delivery, ICS Electronics Corporation will repair or replace at our option this ICS product if any part is found to be defective in materials or workmanship. Labor is included. Return this product to ICS Electronics or other designated repair station, freight prepaid, for prompt repair or replacement. Contact ICS for a return material authorization prior to returning the product for repair.

CERTIFICATION

ICS Electronics Corporation certifies that this instrument was carefully inspected and tested at the factory prior to shipment and was found to meet all requirements of the specification under which it was furnished.

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1

Specifications

1.1 DESCRIPTION

The ICS Electronics Model 4880 IEEE 488 Bus Instrument Coupler (See Figure 1-1) is a general purpose coupler which connects digital instruments to the IEEE 488 Instrument Bus. The 4880 Bus Coupler is manufactured in three standard configurations: 1) as a Talker for connecting measuring instruments to the bus, 2) as a Listener for connecting programmable devices to the bus, and 3) as a Talker/Listener combination. The instrument input and output connections are parallel TTL compatible ports (with latched outputs and gated inputs) that are easily connected to the instrument by simple cables.

The 488 Bus connector is compatible with the electrical and physical requirements of IEEE Specification 488-1975. The 488 Bus uses eight lines for data and eight lines for control and handshake functions. All data is transferred as parallel 8-bit characters under the direction of a controlling device. The 488 Bus concept allows many different instruments to be quickly connected together to form a working system without the use of multiple, special purpose interfaces.

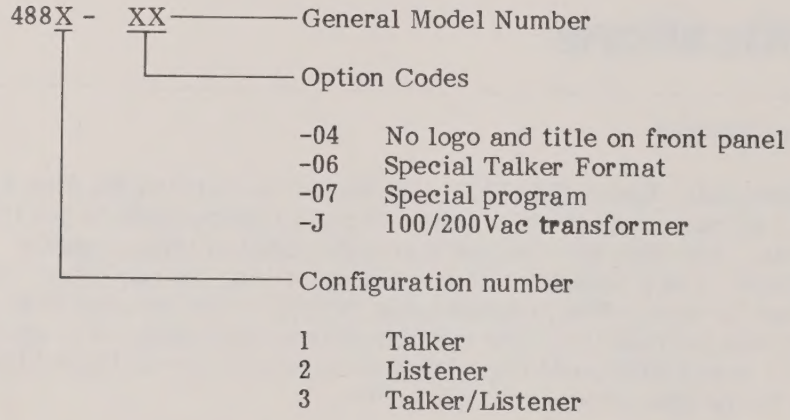


Figure 1-1 Model 4880 Instrument Coupler

1.2 DETAIL SPECIFICATIONS

The following specifications apply in general to all 4880 Series Interfaces. Exact specifications for your model may be found by comparing its model number against the listed specifications.

1.2.1 Model Number Designation



1.2.2 IEEE 488 Bus Interface Functions

Numbers in parenthesis are applicable manual paragraph numbers.

Code	Description	Comments
SH1	Source Handshake	Included
AH1	Acceptor Handshake	Included
T5,TE5	Talker, Extended Talker*	Included (1.2.4)
L4,LE4	Listener, Extended Listener*	Included (1.2.5)
SR1	Service Request	Included
PP1	Parallel Poll	Included*
RL0	Remote, Local	No capacity
DC1	Device Clear	Included (1.2.6.1)
DT1	Device Trigger	Included (1.2.6.2)
C0	Controller	Not Implemented

*Extended address capability can be enabled if parallel poll capability is deleted (3.4.2.6)

1.2.3 IEEE 488 Bus Specifications

Form — Sixteen lines, eight data and eight for control and status messsages. Data transfer is byte serial using three-wire handshake. IEEE 488 command and address messages shown in Table 1-1.

Interface	Driver and receiver circuits TTL compatible. Outputs sink 40mA and drive over 20 meters of cables.
Address Capability	31 Talk/Listen addresses (0 through 30). Talk/Listen configuration uses same address and may not talk to itself. Address may be bypassed and mode selected by using rear panel ONLY Switch.

1.2.4 Talker Format

One to 16 characters for each transmission. Standard shipped format is ten data characters plus a line feed (LF) and carriage return (CR) for each transmission. Input 4-bit BCD or binary data characters are converted to ASCII characters per for the following table:

4-Bit Input Character	ASCII Output Character
0-9	0-9
10	+
11	-
12	. (Period)
13	, (Comma)
14	E
15	(Space)

Talker format and character conversion table are stored in UV erasable PROMs and are user programmable.

1.2.5 Listener Format

Accepts one to ten ASCII characters in the number subset (hex code 30 to 3F). Standard unit outputs four least significant hex bits in each received data character when it detects a comma, line feed or carriage return, or presence of an EOI signal during the last data character.

1.2.6 Special 488 Functions

1.2.6.1 DEVICE CLEAR/SELECTED DRIVE CLEAR/IFC

Listener outputs all zero's or user programmed control code on the output connector, resets all interface signals, and outputs a reset pulse on the J3 Auxiliary control lines. IFC also resets all internal status flags and clears memory.

1.2.6.2 DEVICE TRIGGER

Talker outputs a trigger pulse on the input connector and resets the external data ready flag and instrument inhibit lines.

1.2.6.3 SRQ

Talker generates a Service Request Interrupt (SRQ) when it receives external data if not addressed as a talker. SRQs can be completely inhibited by depressing the front panel SRQ INHIBIT switch. The SRQ signal is reset when 4880 addressed to talk or when serial polled.

1.2.6.4 SERIAL POLL RESPONSE

The 4880 responds to a serial poll by placing a 41-hex character (decimal 65) on the data line if the 4880 SRQ line is on or if the 4880 has data available; otherwise the 4880 responds with a 00-hex character (decimal 0).

1.2.6.5 PARALLEL POLL RESPONSE

The 4880 responds to a parallel poll by placing the Ready Status condition in the bit selected by the PPE command. Bit is a logic '1' if the READY light is on, logic '0' if off. The 4880 requires a minimum ATN off time of 250 microseconds before the parallel poll IDY pulse.

1.2.7 Instrument Inputs

Input	Parallel, 40 bits, one line per bit. Accepts BCD or binary code, see Section 1.2.4. Logic reversal accomplished by grounding Polarity input on J2.
Input Logic Levels	Standard: logic '1' + 2.4 to +5.0 VDC @ -0.02ma logic '0',0 + 0.5 VDC @ 0.36 ma
Ext Data Ready $\overline{\text{Ext Data Ready}}$	Data is loaded into input register after leading edge of External Data Ready (EDR) pulse. The 4880 accepts positive going signals on EDR and negative going signals on $\overline{\text{EDR}}$. The 4880 generates positive and negative going Inhibit signals within 500 nsec. Input data should be stable from the leading edge of the External Data Ready pulse until the Inhibit signals are reset (typically 1500 usec when in talk mode). Minimum External Data Ready pulse width is 1 usec, with same logic levels as above.
Inhibit $\overline{\text{Inhibit}}$	Inhibit signal goes true when the 4880 senses External Data Ready signal and resets when 4880 data input is complete or, within 1 msec if the SRQ INHIBIT switch is depressed. Compliment signal also available on input connector. Both signals can sink 40ma.
Trigger Control $\overline{\text{Trigger Control}}$	Two lines used to provide positive and negative trigger pulses to instrument in response to a device trigger command. Trigger Control is the positive going pulse; $\overline{\text{Trigger Control}}$ is the negative going pulse. Pulse width is 20 usec minimum.

Aux Status	Signal input, used to sense high true instrument ready status. Status input used to operate the READY light.
Polarity	Signal input, high for standard data logic levels; ground for reversed logic levels.

1.2.8 Command Outputs

Formats	Parallel, 4 to 40 bits, one line per bit. Logic reversal accomplished by grounding Polarity input on J3.
Output Logic Levels	Standard logic '1' + 2.4v min @ -0.4 ma logic '0' + 0.5v max @ 8 ma
Output Timing	All data bits transferred to output lines and held until next output word received by the 4880 Controller. Data stable 20 μsec prior to leading edge of Data Strobe.
Data Strobe	Positive going: logic '1' + 2.4v min. @ -0.4 ma logic '0' + 0.5v max. @ 8 ma Pulse Width - 20 μsec minimum
$\overline{\text{Data Strobe}}$	Negative going: logic '1' + 0.5v max. @ 8ma logic '0' + 2.4v min. @ -0.4 ma Pulse Width - 20 μsec minimum
Clear Control $\overline{\text{Clear Control}}$	Same logic levels as Data Strobe and $\overline{\text{Data Strobe}}$. These signals provide a 20 usec clear pulse in response to the IEEE 488 Bus Device Clear or IFC commands.
Device Ready $\overline{\text{Device Ready}}$	Two status inputs (one low true and one high true) are available on the output connector. (See Input logic levels, section 1.2.7). Status inputs 'anded' to operate the READY light.
Aux Status	A high true status input to sense external equipment status. Same logic levels and response as Device Ready signal described above.
Polarity	Signal input, high for high true standard levels; ground for low true logic levels.

1.2.9 Physical Description

CONTROLS	
POWER	Energizes unit.
RESET	Clear internal logic.
SRQ INHIBIT	Disables Talker's service requests.
Address Switch	Rear panel assembly includes 5 address switches, Talk/Listen mode select and the Only switch.
Power Select	Rear panel slide switch selects 115 or 230Vac power.
INDICATORS	
POWER	Illuminates when power is on.
READY	Illuminated when all status lines (1 on Input connector J2 and 3 on Output connector J3) are all in their true states.
TALKING	Illuminated when the 4880s talk address is recognized.
LISTENING	Illuminated when the 4880s listen address is recognized.
DESCRIPTION	
Dimensions	8.5 in. (21.6 cm) wide x 3.5 in. (8.9 cm) high x 11.25 in. (28.6 cm) deep excluding connectors. See Figure 1-2.
Weight	6 pounds (2.7 kgm).
Connectors	Input/output, Amphenol 57-20500; IEEE 488 Bus Interface, Amphenol 57-20240 with metric lock nuts.
Power Requirements	115 or 230Vac + 10%, 48-62Hz, 35 watts max. standard 100 or 200Vac + 10%, 48-62Hz, (-J option) Fuse - 3AG, 1 ampere slo-blow for 100-115Vac - 3AG, 1/2 ampere slo-blow for 200-230Vac
Temperature	-0°C to +50°C operating, -20°C to +70°C non-operating.

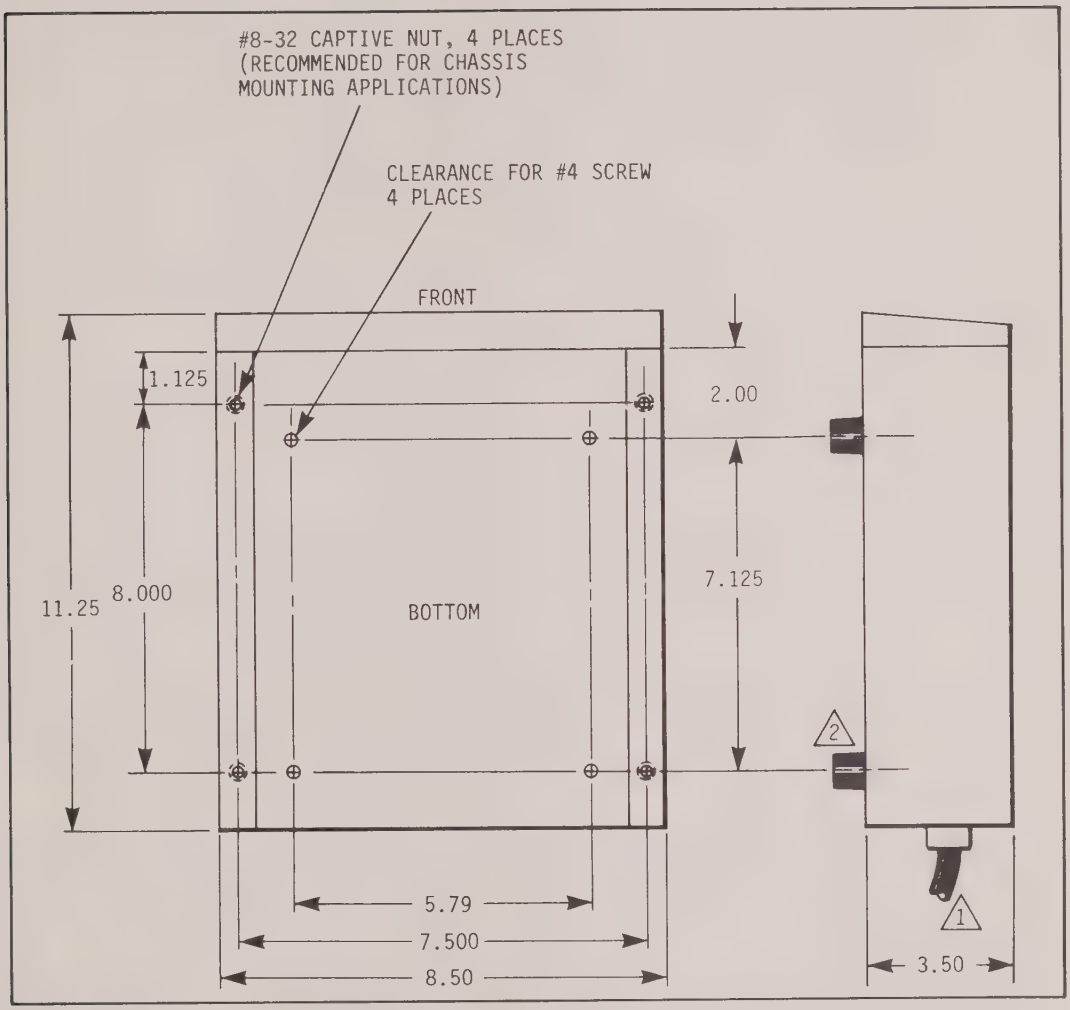


Figure 1-2 4880 Outline Dimension

TABLE 1-1 IEEE 488 COMMAND AND ADDRESS MESSAGES

ASCII — IEEE 488 BUS MESSAGES (COMMANDS AND ADDRESSES) HEX CODES

MSD / LSD	0		1		2		3		4		5		6		7	
	ASCII	MSG	ASCII	MSG	ASCII	MSG[1]	ASCII	MSG[1]	ASCII	MSG[1]	ASCII	MSG[1]	ASCII	MSG	ASCII	MSG
0	NUL		DLE		SP	00	0	16	@	00	P	16	`	MEANING DEFINED BY PCG CODE	p	MEANING DEFINED BY PCG CODE
1	SOH	GTL	DC1	LLO	!	01	1	17	A	01	Q	17	a		q	
2	STX		DC2		"	02	2	18	B	02	R	18	b		r	
3	ETX		DC3		#	03	3	19	C	03	S	19	c		s	
4	EOT	SDC	DC4	DCL	$	04	4	20	D	04	T	20	d		t	
5	ENQ	PPC	NAK	PPU	%	05	5	21	E	05	U	21	e		u	
6	ACK		SYN		&	06	6	22	F	06	V	22	f		v	
7	BEL		ETB		'	07	7	23	G	07	W	23	g		w	
8	BS	GET	CAN	SPE	(	08	8	24	H	08	X	24	h		x	
9	HT	TCT	EM	SPD	)	09	9	25	I	09	Y	25	i		y	
A	LF		SUB		*	10	:	26	J	10	Z	26	j		z	
B	VT		ESC		+	11	;	27	K	11	[	27	k		{	
C	FF		FS		,	12	<	28	L	12	\	28	l		|	
D	CR		GS		-	13	=	29	M	13	]	29	m		}	
E	SO		RS		.	14	>	30	N	14	^	30	n		~	
F	SI		US		/	15	?	UNL	O	15	_	UNT	o		DEL	
	ADDRESSED COMMAND GROUP		UNIVERSAL COMMAND GROUP		LISTEN ADDRESS GROUP				TALK ADDRESS GROUP				SECONDARY COMMAND GROUP			

PRIMARY COMMAND GROUP (PCG)

Notes:

1. Device Address messages shown in decimal
2. Message codes are:
   DCL — Devices Clear
   GET — Device Trigger
   GTL — Go to Local
   LLO — Local Lockout
   PPC — Parallel Poll Configure
   PPU — Parallel Poll Unconfigure
   SDC — Selected Device Clear
   SPD — Serial Poll Disable
   SPE — Serial Poll Enable
3. ATN off, Bus data is ASCII; ATN on, Bus data is an IEEE MSG.

2

Installation

2.1 UNPACKING AND INSPECTION

If shipping carton or instrument is damaged, call carrier immediately. Inspect Controller for damage (scratches, dents, etc.). If unit is damaged or fails to meet specifications notify ICS Corporation or area sales representative immediately. Retain shipping carton and packing material for carrier's inspection. ICS Corporation will make arrangements for unit to be repaired or replaced without waiting for claim against carrier to be settled.

2.2 BENCH OPERATION

The Bus Interface is ready for bench operation when shipped with the exception of setting the rear panel address switch. See Section 3.1.2 for address switch setting instructions.

The unit is equipped with four feet for setting on other instruments. While capable of operation at elevated room temperatures, for best stability and long life, do not place the unit where it will be subjected to undue temperature rises.

2.3 RACK INSTALLATION

Rack installation is feasible only if a rack mounting kit was shipped with the instrument. To convert the unit for rack mounting, do the following:

a. Remove 4880 feet and cover.

b. Slide 4880 in the rack mount tray from the front until front bezel is just outside of rack mount assembly.

c. Turn rack mount tray on its side. Line up 4880 case feet mounting holes with those in the tray. Use furnished screws to fasten the unit in placee.

d. Repeat steps a through c if a second unit is to be installed in the rack mount assembly. If a second unit is not to be installed mount the dummy front panel in its place.

e. Place cover on top of tray and use furnished screws to fasten cover in place.

f. Install rack mount assembly in rack and attach cable to unit(s).

g. To service or adjust units, reverse steps f through c.

CAUTION

ALWAYS REMOVE POWER FIRST BEFORE WORKING ON UNITS.

2.4 POWER CONNECTIONS

The unit may be operated from either 115 or 230Vac, 50 or 60Hz power. A rear panel slide switch selects 115 or 230Vac operation. The units is equipped with a three-prong international power socket which accepts 115Vac American style power cords or 230Vac European style power cords.

Unit is equipped with a 1.0 ampere fuse for 115Vac use. Change fuse to 0.5 ampere for use with 230Vac power.

Optional 100/200Vac transformer available for use in Japan and other Eastern countries.

2.5 IEEE 488 BUS CONNECTIONS

The unit is equipped with a 24-pin connection, J1, which mates with any IEEE 488 Bus Cable. All pin numbers and signals characteristics are per IEEE Specification, IEE Std 488-1975. Signal-pin assignments are listed for reference purposes in Table 2-1.

TABLE 2-1 488 BUS CONNECTIONS (J1)

Pin	Signal	Pin	Signal
1	DIO1	13	DIO5
2	DIO2	14	DIO6
3	DIO3	15	DIO7
4	DIO4	16	DIO8
5	EOI	17	REN
6	DAV	18	DAV Ret
7	NRFD	19	NRFD Ret
8	NDAC	20	NDAC Ret
9	IFC	21	IFC Ret
10	SRQ	22	SRQ Ret
11	ATN	23	ATN Ret
12	Shield	24	Ground

NOTE

J1 mates with an amphenol 57-30240 plug.

2.6 PARALLEL INPUT CONNECTIONS

Units with a talker capability have a rear panel connector, J2, that accepts parallel data. This parallel input path inputs up to 40 bits of data. The unit normally inputs data in BCD or octal format but can be altered to accept data in binary or 8-bit formats. Refer to Section 3.4 for instructions on altering the units data inputting characteristics and Table 2-2 for J2 pin assignments.

2.6.1 External Data Ready

Data is loaded into the bus interface when the external device raises the External Data Ready line. The external Data Ready line must stay high for 1 microsecond or until the Inhibit signal goes high. Data may also be loaded into the unit by dropping the External Data Ready line. To use the External Data Ready line, jumper pin 2 to pin 1 on J2. Data must be stable and remain so until the unit drops the Inhibit lines.

2.6.2 Inhibit

A positive going signal, raised when the unit detects the leading edge of External Data Ready and lowered after the data has been transferred to the interface's memory. May be used to 'hold' the instrument until the data has been read. Inhibit is the compliment of Inhibit. The Inhibit signals are automatically reset by the coupler and the instrument is not held if the SRQ INHIBIT switch is depressed and the coupler is not addressed as a Talker.

2.6.3 Auxiliary Status Input

The Auxiliary Status input signal can be used to tell the bus interface the external device's condition. The coupler monitors this signal to determine if the instrument is ready and to operate the front panel READY Indicator. Auxiliary Status is for high true ready signals and should be pulled high if not used. See Section 3.4 for instructions on modifying the status signal sense.

2.6.4 Trigger Control Outputs

The control outputs are used by the unit to trigger or command the external device to perform its function upon receipt of a 488 Bus Device Trigger command. Trigger Control is normally low and pulses high for 20 usec. Trigger Control is normally high and pulses low for 20 usec.

2.6.5 Polarity

The Polarity input determines the coupler's Input Data logic levels. Tie to +5Vdc for an input logic '1' level of +2.4 to +5Vdc. Ground for an input logic '1' level of 0Vdc.

TABLE 2-2 J2 INPUT PIN ASSIGNMENTS

Signal/Function	Pin No.	Signal/Function	Pin No.
MSD 1	7	MSD-7 1	35
MSD 2	8	MSD-7 2	36
MSD 4	9	MSD-7 4	37
MSD 8	10	MSD-7 8	38
MSD-1 1	11	MSD-8 1	39
MSD-1 2	12	MSD-8 2	40
MSD-1 4	13	MSD-8 4	41
MSD-1 8	14	MSD-8 8	42
MSD-2 1	15	MSD-9 1	43
MSD-2 2	16	MSD-9 2	44
MSD-2 4	17	MSD-9 4	45
MSD-2 8	18	MSD-9 8	46
MSD-3 1	19	Ext Data Ready	2
MSD-3 2	20	$\overline{\text{Ext Data Ready}}$	6
MSD-3 4	21		
MSD-3 8	22	Inhibit	3
		$\overline{\text{Inhibit}}$	4
MSD-4 1	23		
MSD-4 2	24	Aux Status*	47
MSD-4 4	25		
MSD-4 8	26	Polarity**	48
MSD-5 1	27	Trigger Control	49
MSD-5 2	28	$\overline{\text{Trigger Control}}$	50
MSD-5 4	29		
MSD-5 8	30	+5Vdc	5
MSD-6 1	31	Ground	1
MSD-6 2	32		
MSD-6 4	33		
MSD-6 8	34		

NOTES

1. *Connect to +5Vdc if not used.
2. **Tie to +5Vdc or gnd, see 2.6.5.

2.6.6 Input Data

Data is normally coded in BCD or binary form and inputted in 4-bit bytes as shown in Table 2-3. Binary data can be divided into groups of three bits and inputted as octal numbers by grounding the unused eight weight input lines. Each group of four bits is internally converted into an ASCII character before being transmitted over the IEEE Bus. The standard talker converts BCD or HEX codes into ASCII characters as shown in Table 2-3).

To make other conversions see Section 3.4 for instructions on altering the Talker Conversion table.

TABLE 2-3 STANDARD TALKER INPUT CODE CONVERSIONS

INPUT VALUE	INPUT CODE	ASCII OUTPUT	INPUT VALUE	INPUT CODE	ASCII OUTPUT
0	0000	0	8	1000	8
1	0001	1	9	1001	9
2	0010	2	10	1010	+
3	0011	3	11	1011	-
4	0100	4	12	1100	.
5	0101	5	13	1101	,
6	0110	6	14	1110	E
7	0111	7	15	1111	Space

2.6.7 Input Cable Design

To design an input cable, first list all data signals in column form starting with the most significant digit. Make the list in groups for four bits and give single signals such as sign, their own 4-bit group. In the next column, list the instruments output connector pin numbers. In the third column, list the coupler's corresponding input pin numbers. Refer to Table 2-3 for the Bus Interfaces input codes (for single signals like sign) and jumper any pins requiring logic 1 to +5Vdc and logic 0 to ground. Connect the instruments measurement complete signal (often called print or data ready) to the coupler's proper polarity External Data Ready signal. Connect the Auxiliary Status input to the instrument or jumper to +5Vdc as described in paragraph 2.6.3. Use the polarity signal to define the data logic levels as described in paragraph 2.6.5. A Sample Input Cable is shown in Table 2-4..

CAUTION

RECHECK LOGIC 1 AND LOGIC 0 DATA BIT JUMPERS AFTER SETTING POLARITY JUMPER.

TABLE 2-4 SAMPLE INPUT CABLE

Instrument Signal	Instrument Pin No.	4880 Input Pin No.	4880 Signal
Minus	A	7	MSD 1
-	-	8	MSD 2
-	-	9	MSD 4
-	-	10	MSD 8
100's 1	B	11	MSD-1 1
-	-	12	MSD-1 2
-	-	13	MSD-1 4
-	-	14	MSD-1 8
10's 1	C	15	MSD-2 1
" 2	D	16	MSD-2 2
" 4	E	17	MSD-2 4
" 8	F	18	MSD-2 8
1's 1	6	19	MSD-3 1
" 2	4	20	MSD-3 2
" 4	5	21	MSD-3 4
" 8	K	22	MSD-3 8
-		2	EDR
Print	N	6	$\overline{\text{EDR}}$
		3	Inhibit
Hold	P	4	$\overline{\text{Inhibit}}$
		47	Aux #1
		48	Polarity
Common	R	1	Ground
		5	+5Vdc

NOTE

Pin to pin interconnection lines such as A to 7 are not shown for clarity.

2.7 PARALLEL OUTPUT CONNECTIONS

Units with Listener capability provide a 40-bit parallel output word on rear panel connector J3. The output word is driven by 74LS75 type latches that are loaded each time the interface receives a new message from the IEEE 488 Bus. The data outputted is derived by extracting the four least significiant bits from each ASCII 30-hex(0011 0000) through 3F(0011 1111) 8-bit character. The 4-bit characters are assembled in memory and outputted only when a message terminating character is received. The assembled word is outputted MSD first so a two-character message only changes the first eight bits and a ten-character message changes the whole 40 bits.

Message transfer is under control of the simple handshaking signals described below. Refer to Section 3.4 for instructions on changing the message termination characters and Table 2-5 for output pin assignments.

2.7.1 Data Strobe Outputs

The Data Strobe line is raised after a new message has been loaded into the output latches. The Data Strobe drops after 20 μsec. $\overline{\text{Data Strobe}}$ is the compliment of Data Strobe.

2.7.2 Device Ready Input

Device Ready and $\overline{\text{Device Ready}}$ are input signals which let the unit know if the external device is ready to receive additional data. These lines are tested to generate the instrument ready signal and operate the front panel READY indicator. Device Ready is for a high true signal and should be pulled high if not used. $\overline{\text{Device Ready}}$ is for a low true signal and should be grounded if not used.

2.7.3 Aux Status Input

Aux Status is an additional input signal which monitors the external device's status. Operation is identical to Device Ready signal described above. Pull Aux Status input to +5Vdc if not used.

2.7.4 Polarity

The Polarity input determines the polarity of the output data word. Pull to +5Vdc for an output logic '1' of +2.4 to +5Vdc or tie to ground for a logic '1' = 0Vdc.

2.7.5 Clear Control Outputs

Clear Control and $\overline{\text{Clear Control}}$ are spare output signals that can be used to reset or clear the external device in response to the IEEE 488 Device Clear, Selected Device Clear, or IFC commands. Clear Control is normally low and pulses high for a minimum of 20 μsec. $\overline{\text{Clear Control}}$ is the compliment of Clear Control.

TABLE 2-5 J3 OUTPUT PIN ASSIGNMENTS

Signal/Function		Pin No.	Signal/Function		Pin No.
MSD	1	13	MSD-7	1	12
"	2	14	"	2	43
"	4	15	"	4	42
"	8	16	"	8	41
MSD-1	1	11	MSD-8	1	34
"	2	10	"	2	35
"	4	9	"	4	37
"	8	8	"	8	36
MSD-2	1	2	MSD-9	1	33
"	2	3	"	2	31
"	4	4	"	4	32
"	8	6	"	8	30
MSD-3	1	38	$\overline{\text{Data Strobe}}$		22
"	2	39	Data Strobe		23
"	4	40			
"	8	7	$\overline{\text{Clear Control}}$		25
			Clear Control		24
MSD-4	1	29	$\overline{\text{Device Ready*}}$		21
"	2	26	Device Ready#		50
"	4	27			
"	8	28	Aux Status*		49
MSD-5	1	47	Polarity Control**		48
"	2	46			
"	4	45			
"	8	44	+5Vdc		5
MSD-6	1	20	Ground		1
"	2	19			
"	4	18			
"	8	17			

NOTES

1. J3 mates to an Amphenol 57-3050 plug.
2. *Tie to +5 Vdc if not used.
3. #Ground if not used.
4. Tie to +5Vdc or gnd, see 2.7.4.

2.7.6 Output Cable Design

The design of the output cable is directly related to the output message format and the signals needed to drive the external device. If the message format is fixed, it can be listed in column form, adjacent to the interface's output data signal names. Start with MSD first as shown in the example in Table 2-6. List the output pin numbers from Table 2-5, as column 3. Next list the corresponding external device signal names and pin numbers. Add the control signals and the cable is made by wiring the two columns of pin numbers together. Add jumpers for the unused control signals as required.

If the message format is not yet chosen, list just the coupler's output signal names and pin numbers as in columns 2 and 3 of Table 2-6. List the device signals in the logical sequence, putting the more commonly changed functions first. Arrange the signals in groups of four so that one output digit controls only one function if possible. List the corresponding external device pin numbers for the signals and complete the cable as described above.

TABLE 2-6 SAMPLE OUTPUT CABLE

1 Message Format Assignments		2 Output Signal	3 Output Pin No.	4 Device Pin No.	5 Device Signal	
Function	1	MSD 1	13	A	Measure	AC
"	2	MSD 2	14	B	"	DC
"	4	MSD 4	15	C	"	Ohms
"	8	MSD 8	16	D	"	Kohms
Polarity	+	MSD-11	11	E	Polarity	+
"	-	MSD-12	10	F	"	-
		MSD-14	9			
-		MSD-18	8		-	
-					-	
Range	10^0	MSD-21	2	I	Range	1
"	10^1	MSD-22	3	J	"	10
"	10^2	MSD-24	4	K	"	100
"	10^3	MSD-28	6	L	"	1000
Filter		MSD-31	38	M	Filter in	
-		MSD-32	39		-	
-		MSD-34	40		-	
-		MSD-38	7		-	
		Data Strobe	22	R	Load	
		$\overline{\text{Data Strobe}}$	23			
		Device Ready	21	S	Local*	
		$\overline{\text{Device Ready}}$	50			
		Aux Status	49			
		Polarity Con#	48			
		+5Vdc	5			
		Ground	1			

NOTES

1. Pin to pin interconnection lines such as 13 to A are not shown for clarity.
2. *Grounded by instrument if in local
3. #Grounded for low true data outputs

3

Operation

3.1 CONTROLS

3.1.1 Front Panel Controls

POWER — An alternate action push button that applies AC power to the interface. In is ON.

RESET — Momentary push button that resets the internal logic, input data ready flag and sets the output command word to its initial conditions.

SRQ INHIBIT — An alternate action push button that prevents Talker models from generating service requests each time an instrument's EDR signal is detected. INHIBIT is In.

3.1.2 Address Switch

The address switch assembly sets the Coupler address and establishes the Talker or Listen Only modes. The address switch is miniature, switch assembly with eight rocker switches that is located on the rear panel. From left to right the switch positions are address bits 2^0,2^1,2^2,2^3,2^4, Talk, Listen and Only. See Figure 3-1.

To set the Coupler address, pick an unused bus address between 0 and 30 decimal. Convert the address to binary and write it left to right putting the LSB on the left. Set the five address switches to the binary value. Top in is a logic '1', i.e., address 3 becomes:

1	2	3	4	5
1	1	0	0	0

Refer to Section 3.4.2.6 for instructions on setting the secondary address. To set the Coupler to a Talk or Listen Only mode, set the T (Talk) or L (Listen) switch and the O (Only) switch on. Position the unused T or L switch off. Press RESET to clear unit after changing the T, L or O switches.

NOTE

The O (Only) switch must be set to off if the interface is to be addressed by the bus controller.

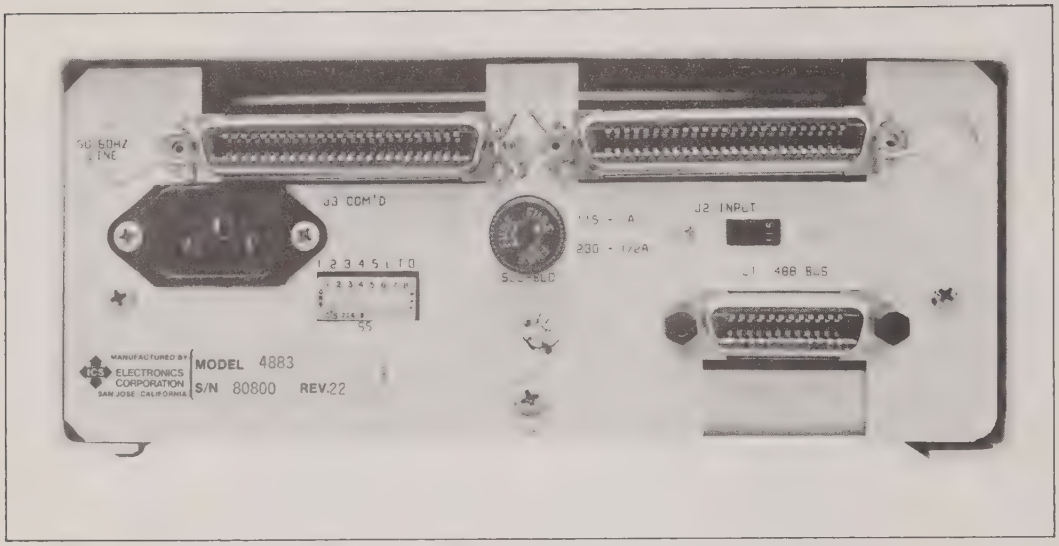


Figure 3-1 4880 Rear Panel

3.1.3. 115/230 Switch

The Rear Panel 115/230 Switch adjusts the power supply for the AC line voltage. Check the switch setting prior to using the instrument. Use a small screw driver to slide the switch until 115 or 230 appears through the slot in the rear panel. For 115Vac operation, use the 1 ampere fuse supplied with the unit. For 230Vac operation, substitute an 0.5 ampere 3AG fuse. With the optional 110/200Vac transformers, the 115 position selects 100Vac and the 230 position selects 200Vac operation. Remove power cord before switching.

3.2 OPERATING INSTRUCTIONS

The following instructions are for a Talker/Listener combination unit. For Talker or Listener configurations, skip those instructions which obviously do not apply to your unit.

3.2.1 Pre-Operation Setup

Before using the 4880 IEEE Bus Interface, design and fabricate the instrument interface cables. Add the mating connector from your instrument to the 80103810 Input and 80103820 Output open end cables or refer to Section 2.6 and 2.7 for complete cable design instructions. Use these cables to connect the instruments to the Interface connectors J2 and J3. Connect dummy plugs to unused J2 and J3 connectors to jumper the unused status inputs per Sections 2.6 and 2.7.

NOTE

Dummy plugs with the necessary jumpers are included with each coupler.

Use an IEEE 488 Bus cable to connect the interface to the bus controller or to another bus compatible instrument. Set the address and power switches per Sections 3.1.2 and 3.1.3. Plug the power cord into an AC power receptacle.

3.2.2 Operation

Depress the POWER switch to turn the 4880 on. The POWER indicator will come on. Place the SRQ INHIBIT switch in the Off position (switch out) and apply power to the instruments connected to the Interface. The instruments' controls should be set for remote operation and control. The READY light will come on to indicate that the instruments connected to the Interface are in their normal or ready state. If the READY light is not On, check the instruments for any error conditions and the cable wiring per Sections 2.6 and 2.7. Do not proceed if the READY light is off since the 4880 will return a logical '0' status response to a parallel poll.

The Controller should send an IFC command to reset the Interface. Messages sent to the instrument being controlled should be proceded by setting the interface to Listen (my listen address state). The Controller should take the Interface out of the listen mode after the instrument is programmed to avoid accidentially changing its output as data is transmitted over the bus. The LISTENING indicator is on while the Interface is in the Listen mode.

The Interface will detect the talking instrument's "external data ready" signal and will generate a Service Request by pulling the IEEE Bus SRQ signal low if not in the talk mode. The Controller may set the serial poll mode with the 'SPE' command and perform a serial poll to find which device requested service.

The Controller then terminates the serial poll mode with an 'SPD' command and puts the Interface in the Talk mode so the Interface can transmit the data onto the bus. When the data transmission is complete, the Interface drops the inhibit lines to the instrument, so that it can make another measurement. If the instrument is being operated in the 'external trigger mode', the Controller will have to issue the Device Trigger command to start a new measurement cycle. The TALKING indicator is on while the Interface is in the Talk mode. The Service Requests can be elminiated by placing the SRQ INHIBIT switch in the Inhibit position (switch in).

The Controller can perform a parallel poll at any time to check on the status of the 4880's READY indicator. This indicator combines the four instrument status signals into one status bit. The Controller performs the parallel poll by sending the PPC and PPE commands to configure the coupler's response message followed by sending an EOI with an ATN. The 4880 detects the presence of the EOI and ATN signals and outputs the Ready status bit on the data line indicated by the configure command. The 4880 detects the parallel poll disable command and resets the configure bit pattern to zero. See Section 3.5.1 before performing a parallel poll.

3.3 USER PROGRAM AIDS

This section contains program steps designed to assist the user in getting the 4880 Bus Interface Coupler to operate with the Bus Controller. The typical Bus Controller may be an intelligent terminal, (Tektronix 4051), a programmable calculator (HP 9825, Wang 2200) or a custom controller (includes minicomputer interfaces).

While the following programs are written for the Tektronix 4051 Terminal and the HP 9825 calculator, they can easily be modified for use on most programmable calculators and custom controllers. Paragraph 3.3.1 contains sample Tektronix 4051 programs and paragraph 3.3.2 contains sample HP 9825 programs.

3.3.1 Tektronix 4051 Programs

3.3.1.1 BASIC TALK PROGRAM

Program inputs data from the 4880 Coupler and displays it on the 4051 CRT. Use with single address couplers.

Initial Steps: Connect the Coupler to a device which generates input data or connect dummy input to 4880 rear panel connector, J2. Set the rear panel address switches to the desired address and compute the Tektronix talk decimal address valule by adding 64 to the turned on ad dress switch decimal values as follows.

Talk Decimal address:
$= 64 + 2^0 + 2^1 + 2^2 + 2^3 + 2^4$
$= 64 + 0 + 0 + 0 + 0 + 16$
$= 80$ for octal address 20

Program:
```
100 - WBYTE @ (decimal address):
```
becomes
```
100 - WBYTE @ 80:
110 - RBYTE A,B,C,D,E,F,G,H,I,J,K
120 - PRINT A,B,C,D,E,F,G,H,I,J,K
130 - END
```

The program uses letters A through K to input individual characters in the standard 4880 Talker format of ten data characters, Carriage Return and Line Feed. The 4051 will ignore the Line Feed following the Carriage Return. Modify the above program for non-standard formats.

Enter 'RUN' and load a reading from the instrument into the 4880 (if by hand, momentarily ground J2 pin 2 to J2 pin 1). The 4880s TALKING light will come on and the data will appear in column format on the 4051s CRT as shown in Figure 3-2.

```
100 - WBYTE @ 80
110 - RBYTE A,B,C,D,E,F,G,H,I,J,K
120 - PRINT A,B,C,D,E,F,G,H,I,J,K
RUN - 100

48   49   50   51
52   53   54   55
56   57   13
```

Figure 3-2 Display for Sequential 0 Through 9 Ten Digit Input

3.3.1.2 HIGH LEVEL TALK PROGRAM

Program uses 4051 Input command to input data and display it on the 4051 CRT. Use with single or extended address couplers.

Initial Steps: Connect the coupler to a measuring instrument or to a dummy data source as described in Section 3.3.1.1. Compute the Tektronix system address by adding the turned on address switch decimal values as follows:

System Address:
$= 2^0 + 2^1 + 2^2 + 2^3 + 2^4$
$= 0 + 0 + 0 + 0 + 16$
$= 16$ for octal address 20

Program:
```
200 - INPUT @ (Address), 32:A
```
becomes
```
200 - INPUT @ 16, 32:A
210 - PRINT A
220 - END
```

A is a string variable and will input all data until it receives a carriage return. The 32 in line 200 causes the 4051 to delete the secondary address message since the standard 4880 decodes the secondary address message as a Parallel Poll Unconfigure command. Refer to Section 3.4 for instructions on converting the 4880 to recognize the secondary address. Enter 'RUN' and load data into the 4880 Coupler. The 4880s TALKING light will come on and the data will appear on the 4051's CRT in floating point format.

i.e., "1.23456789E+8" for the same sequential ten digits as in 3.3.1.1.

3.3.1.3 SQR INTERRUPTS

If the data is being generated by a free running device, there is a good chance that the 4880 could have received the data before the 4051 executed the RUN command. In this case, the 4880 will set the service request (SRQ) line low, indicating that it has a message for the terminal. The 4880 will automatically reset the SRQ line when it is allowed to 'talk' by the Controller. However, the 4051 will sense the SRQ line and issue an error statement like:

"NO SRQ ON UNIT IN LINE 200 - MESSAGE NUMBER 43"

This error message indicates the user failed to tell the 4051 what to do with the service request. The problem can be gotten around by adding the following statements to the program:

```
100 - ON SRQ THEN 200          in main body of program
110 -
.
PROGRAM OR LOOP TO 100
.
```

```
.
200 - INPUT @ 16, 32:A          Perfoms input operation
210 - PRINT A                   and returns to main pro-
220 - RETURN                    gram
```

If there are two or more 4880s on the bus, the program can be written to find which device requested service and answer it. To do this the Controller conducts a serial poll of the possible talkers on the bus. The 4051 program to do the serial poll is:

```
100 - ON SRQ THEN 300           SRQ enable
110
.
PROGRAM OR LOOP TO 110
.
200 - INPUT @ 16, 32:A          Device 16 service routine
210 - PRINT A
220 - RETURN

300 - POLL C,D: 16;17           Poll devices 16 and 17.
310 - GO TO C OF 200, 320       Go to 200 for device 16,
320 - RETURN                    320 for device 17.
```

3.3.1.4 HIGH LEVEL LISTEN PROGRAM

Program uses high level print command to output data. Compute the instrument address as done in 3.3.1.2.

Program:

```
200 - PRINT @ 16, 32: "0123456789"
210 - END
RUN
```

This program outputs the ten digits and lets the 4051 do the address and number conversion. Note that some early 4051 terminals hold the EOI line on while outputting the numbers and the 4880 coupler responds by outputting each characater as the MSD digit on the J3 connector as it is received, rather than, all at once as should be done.

3.3.1.5 DEVICE TRIGGER COMMANDS

The 4880 accepts the Bus Device Trigger command and pulses the 4880 Control output lines to trigger an external device. The following instruction causes the Textronix 4051 to duplicate the HP 9825 'trg' instruction for address number 16.

```
110 - WBYTE @ 63, 48, 08, 63:
```

3.3.2 Hewlett-Packard 9825 Calculator Programs

The HP 9825 calculator is programmed in HPL Language which is similar in many respects to the Tektronix basic language. However, the user should keep the following differences in mind: The HP higher level 488 bus instructions do not re-

turn the devices on the 488 bus to the "unlisten" or "untalk" state as do the corresponding Tektronix commands. All talk sequences should be terminated with an "untalk" command. Also, the HP commands automatically end output transmissions (i.e., wrt) with a line feed and carrage return rather than with the EOI signal as does the Tektronix terminal. The HP 9825 expects the data input to be terminated by a line feed character.

The following examples were written for use on a HP 9825 calculator equipped with an Extended I/O ROM and are intended to assist the user in quickly getting his system on line. The same programs can be converted for use on an HP 9830 calcualtor. The two main conversion rules are: delete the 7 in the "cmd" instructions and rewrite the arithmetic operations. Check your 9830 manual for the equivalents for the other instructions used in the sample programs.

3.3.2.1 HP ADDRESS TEST PROGRAM

Program, shown in Figure 3-3, outputs command characters to put the 4880 Coupler in the Talk and Listen states. Program demonstrates the 'cmd' statements and checks address operation.

Initial Steps: Connect the coupler to the Calculator 488 Bus Adapter cable. Plug the adapter into the calculator. Set the 4880 rear panel address switches to the desired address. For address 04 Hex, set all switches off and bit 3 switch on.

```
0:  1-Device 04
 addr test":
1:  cmd 7;"?_"
2:  wait 50
3:  cmd 7;"$"
4:  wait 50
5:  cmd 7;"D
6:  wait 50
7:  sto 1
8:  end
*b18:
```

Figure 3-3 HP Address Check Program

NOTES

1. '$' is Listen 04 address
2. 'D' is Talk 04 address
3. '?-' is Unlisten, untalk

Press 'RUN'. The program sequentially clears on the 4880 lights, turns the LISTENING light on and then the TALKING light on in 0.5 second steps. Program repeats until the 'STOP' button is pressed.

3.3.2.2 BASIC HP READ - WRITE PROGRAM

Program, shown in Figure 3-4, outputs a fixed number to the 4880 Coupler, reads a value from the 4880 Coupler and displays what was read. Program is used with single address 4880 Couplers.

Initial Steps: Connect the coupler's parallel connectors to dummy BCD inputs and a display device. Connect the coupler to the Calculator 488 Bus Adaptor cable. Plug the adapter into the calculator. Set the 4880 rear panel address switches to the desired address. For address 04 Hex, set all swtiches off and switch on 3.

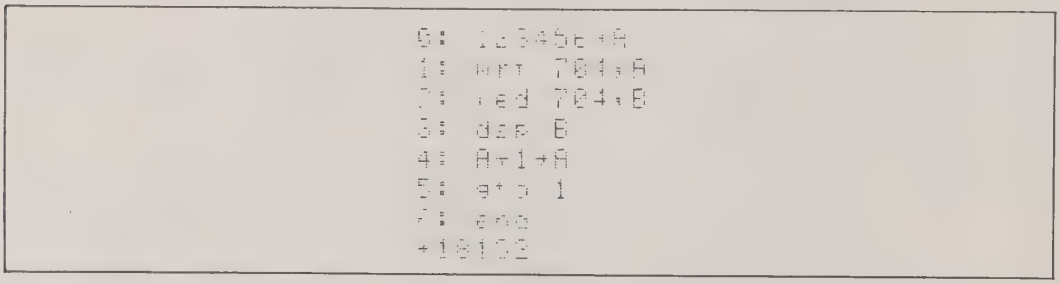


Figure 3-4 HP Basic Read/Write Program

The 9825 uses code 7 in the 'wrt' and 'red' instructions to address the 488 Bus adapter. Press 'RUN'. The calculator will address the 4880 as a listener and output the value A to it. The number 12345600000 will appear on the 4880 output lines. The calculator will put the 4880 into the Talk mode. Any data entered into the 4880 will be transferred to the calcualtor and displayed. The program repeats, incrementing the output number until the 'STOP' button is pressed. Data is entered into the 4880 when the coupler detects a level change on the External Data Ready input line.

3.3.2.3 HP SRQ INTERRUPTS

If the data is being inputted into the 4880 by an external device, the 4880 could be ready to send data before the calculator puts the 4880 into the Talking state. Subsequent 4880 data inputs would be lost unless the first data entry was ready by the calculator. The following example shows the use of the SRQ interrupt to the input data, see Figure 3-5.

Initial Steps Connect the calculator and coupler as described in Section 3.3.2.2. Write an interrupt enable command in the main programbody. Write a special data handling routine to input the data. Set the 4880 address to 04 Hex.

Program

```
0: "2-DEVICE 04
 SERIAL POLL
 TEST":
1: 0→A
2: oni 7,"SRQ"
3: eir 7
4: wait 500
5: gto 4
6: end
7: "SRQ":rds(704
 )→S
8: if S#65;gto
 "DSP"
9: red 704,B
10: wrt 704,B
11: "DSP":cmd 7,
 "?_"
12: prt B
13: dsp S,B
14: wait 500
15: eir 7;iret
*3850
```

Printout

```
1234567890.00
2345678901.00
3456789012.00
4567890123.00
5678901234.00
6789012345.00
7890123456.00
8901234567.00
9012345678.00
 1234567890.00
1234567890.00
```

Figure 3-5 HP SRQ Interrupt Program

The 4880 generates an interrupt when it receives data. The interrupt causes the program to branch to label SRQ and serial poll the coupler. If the serial poll response is 65 decimal (41 hex) the program will read the data and display it. The untalk command (cmd 7, "_") is mandatory to set-up the 4880 for the next interrupt. The program displays the serial poll response and the data before returning from the interrupt. The printout was made by varying the data inputted into the 4880.

3.3.2.4 HP PARALLEL POLL

The HP 9825 calculator program can use the parallel poll instructions to test the Interface READY indicator (and therefore the device status). Data can then be transferred to or from the device depending upon the condition of the status bit.

Intital Steps: Connect the calculator and coupler as described in Section 3.3.2.2. Set the 4880 address to 04 hex. Set the internal E jumper to the E-F position to enable the parallel poll logic (see Section 3.5.1). Connect a switch to one of the status inputs to select either +5Vdc or ground.

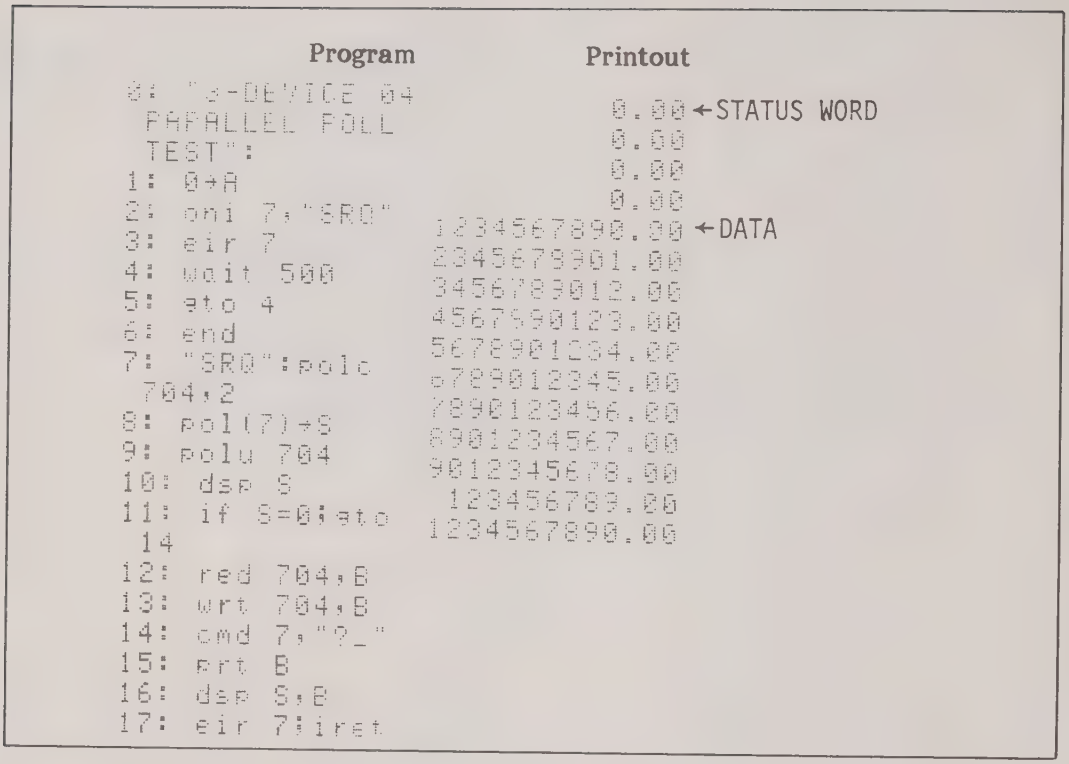


Figure 3-6 HP Parallel Poll Program

The program samples, displays, and prints the status bit once every two seconds. Instruction "polc 704,2" configures the 4880 to return the status bit in bit 2. The program prints and outputs data if the status is equal to 4 (all status lines true) and only prints the status word when it is unequal to 4.

3.4 INTERNAL PROGRAM CHANGES

The user can modify the 4880s performance by altering the contents of various program tables stored in a UV eraseable PROM. User alterable tables include: initial output command word, status line definitions, listen output command characters, input data conversion code and talk output format. General directions for modifying the PROM are given in Section 3.4.1 and specific table locations and definitions are covered in Section 3.4.2.

3.4.1 4880 PROM Alternation Instructions

Altering the 4880s PROM, requires the use of a PROM Programmer that can erase and program 2708 PROMs and a minimum of two spare 2708 PROMs. Do not disassemble the Interface until you have located a PROM Programmer and have the spare PROMs. If a PROM Programmer is not available locally, you can request a PROM programmed to your exact configuration directly from ICS. Perform the following steps to change or alter the 4880 PROM.

a) Disconnect all cables and power cord from the 4880 Interface.

b) Remove the five screws holding the case to the bottom plate (four on the bottom, one in the rear). Tilt the unit to slide the electronics assembly out the rear.

c) The 2708 PROMs are located on the right rear side of the main (lower) board, see Figure 3-7. Locate the PROM to be change by comparing its higher order starting address with that marked on the PC board adjacent to the PROM socket. PROM 00 holds addresses 0000 to 03FF, PROM 08 holds addresses 0800 to 0BFF. Use a flat bladed tool to pry the PROM evenly up out of its socket. Skip d) if the PROM is to be replaced by a factory furnished PROM.

d) List the section of the PROM to be changed and verify that it matches the tables given in Section 3.4.2. Make the changes by duplicating the good portions of the PROM onto a new PROM. Program in all changes and check by listing them back. Verify that all other portions of the original PROM have been duplicated on the new PROM. Do not erase the original PROM.

e) Place the new PROM back in the socket. Line the PROM pins up carefully with the socket and use a rocking motion to push the PROM into the socket. Check to see that all pins went into the socket and that none were bent underneath.

f) Reverse steps b) and a) to close the unit. Make sure the switch caps are through the opening in the front panel before tightening the rear panel holding screws.

g) Erase the original PROM only after thoroughly testing the interface.

3.4.2 PROM Program Tables

This Section covers the 4880 PROM Program Tables that can be modified by the user to change the 4880s operation. All data is in hex code format, and each character has two hex digits or eight bits. Bit 1 or the LSB is on the right. Logic '1' produces a high signal unless otherwise noted. User alterable characters are labeled UA.

3.4.2.1 INITIALIZATION TABLE

The Initializaton Table (see Table 3-1) sets up the intial conditon of all output signals and memory flags. User alterable areas include initial output command word, control lines and GP-IB signals.

Power on clear and front panel RESET button clears the coupler's memory before loading the Initialization Table. Device clear and Selected Device Clear commands only load the Initialization Table into memory.

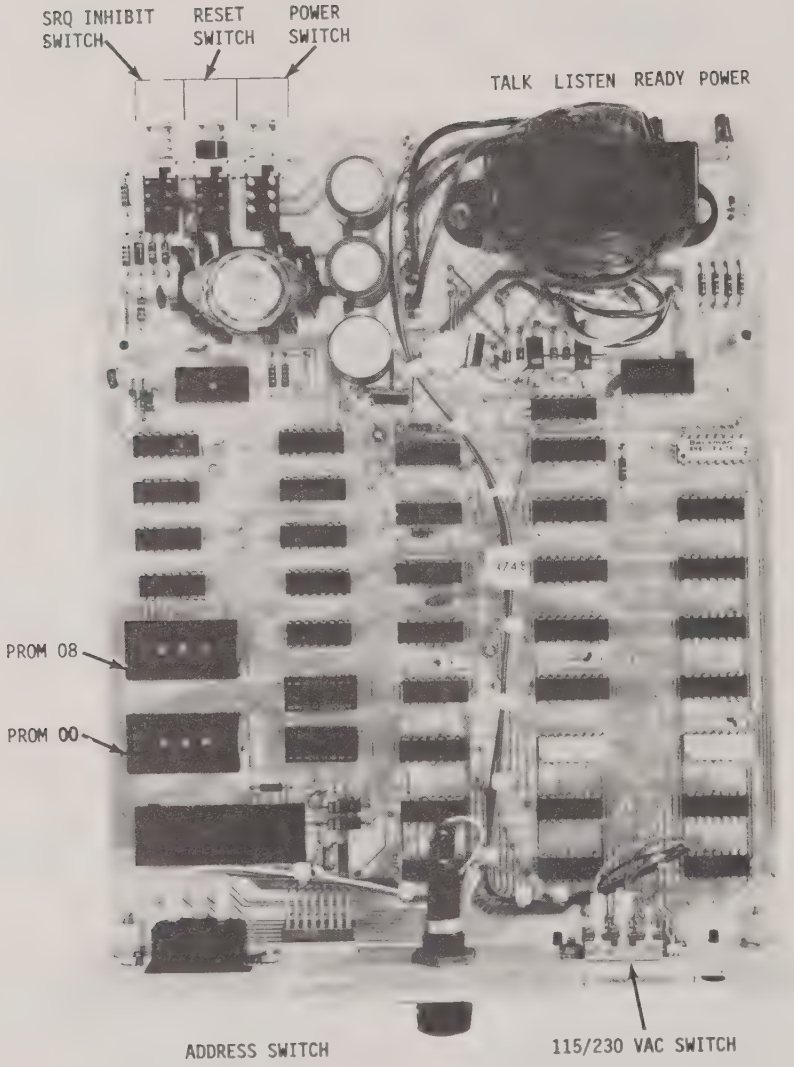


Figure 3-7 4880 Main Board Component Locations

TABLE 3-1 INITIALIZATION TABLE

PROM	Address	Code		Description
00	03B3	0B		
00	B4	1F		
00	B5	04		
00	B6	0A	UA	Numbers of Output Characters in Buffer
00	B7	00	UA	Digit #1 (J3-MSD) (Note 4)
00	B8	00	UA	Digit #2
00	B9	00	UA	Digit #3
00	BA	00	UA	Digit #4
00	BB	00	UA	Digit #5
00	BC	00	UA	Digit #6
00	BD	00	UA	Digit #7
00	BE	00	UA	Digit #8
00	BF	00	UA	Digit #9
00	C0	00	UA	Digit #10 (J3-LSD)
00	C1	01		
00	C2	07		
00	C3	05		
00	C4	06	UA	Output Strobes (Note 1)
00	C5	02		
00	C6	06		
00	C7	06		
00	C8	02	UA	Control Signals (Note 2)
00	C9	00		EDR F/F Reset command
00	CA	06		
00	CB	02		
00	CC	07		
00	CD	00	UA	GP-IB Data Outputs
00	CE	00	UA	GP-IB Signal Outputs
00	CF	80		Output Ena F/F Set Command
00	D0	00		
00	D1	00		
00	D2	00		Lites (Note 3)
00	03D3	00		Terminate Code

NOTES

1. Bit 1 = Data Strobe, Bit 2 = $\overline{\text{Data Strobe}}$
   Bit 3 = $\overline{\text{Aux Control}}$, Bit 4 = Aux Control

2. Bit 1 = Control, Bit 2 = $\overline{\text{Control}}$

3. Bit 1 = Ready, Bit 2 = Listen, Bit 3 = Talk
   Bit 4 = Parallel Poll Enable

4. Data is in 4 LSB's, i.e. 07 outputs 0111

3.4.2.2 STATUS INPUTS TABLE

The Status Inputs Table (Table 3-2) contains the secondary address code plus the condition of the J2 and J3 status lines when they are in the 'Ready' condition. Changing a status line bit from a logic '1' to a logic '0' converts the corresponding status input from a high true to a low true signal.

TABLE 3-2 STATUS INPUTS

PROM	Address	Code	Description
00	0390	00 UA	Secondary Address
00	91	02 UA	Input Status, Bit 2 = J2 Aux Status
00	0392	05 UA	Output Status, Bit 1 = J3 $\overline{\text{Device Ready}}$
			Bit 2 = J3 $\overline{\text{Device Ready}}$
			Bit 3 = J3 Aux Status

NOTE

For Model 4882, 0391 code = 00
For Model 4881, 0392 code = 00

3.4.2.3 LISTEN TABLE

The Listen Table (Table 3-3) contains the ASCII characters used as data deliminators for data received from the IEEE 488 Bus. Detecting a deliminator causes the coupler to transfer any prior received data to the output connector, J3. Different deliminators may be selected by substituting the proper ASCII code in the table.

TABLE 3-3 LISTEN DELIMITERS

PROM	Address	Code	Description
00	03F5	0D UA	Carriage Return
00	F6	CC	
00	F7	02	
00	F8	0A UA	Line Feed
00	F9	CC	
00	FA	02	
00	FB	2C UA	Comma
00	FC	CC	
00	FD	02	
00	FE	A7	
00	03FF	02	

3.4.2.4 TALK CONVERSION TABLE

The Talk Conversion Table (Table 3-4) contains the ASCII codes outputted for each of 16 possible input codes on connector J2. The ASCII character codes and J2 input codes are both in Hex Form.

TABLE 3-4 TALK CONVERSION TABLE

Prom	Address	Input Code	Talk Code	ASCII Output Character
00	03D4	0	30 UA	0
	D5	1	31 UA	1
	D6	2	32 UA	2
	D7	3	33 UA	3
	D8	4	34 UA	4
	D9	5	35 UA	5
	DA	6	36 UA	6
	DB	7	37 UA	7
	DC	8	38 UA	8
	DD	9	39 UA	9
	DE	A	2B UA	+
	DF	B	2D UA	-
	E0	C	2E UA	. (period)
	E1	D	2C UA	, (comma)
	E2	E	45 UA	E
00	03E3	F	20 UA	Space

3.4.2.5 TALK FORMAT TABLE

The Talk Format Table (Table 3-5) controls the format of the data message put on the bus during the talk mode. Data characters are coded as an 80 in the table, symbol characters start with a 0 in bit 8, (i.e., 0A for CR) and end of message is indicated by a 19. (See Table 3-5.). End of message is a non-transmitted character used internally to end the data message.

TABLE 3-5 TALKER FORMAT TABLE

Prom	Address	Format Talk Code		Description
00	03E4	80	UA	Word 1 = Data
	E5	80	UA	2
	E6	80	UA	3
	E7	80	UA	4
	E8	80	UA	5
	E9	80	UA	6
	EA	80	UA	7
	EB	80	UA	8
	EC	80	UA	9
	ED	80	UA	10 = Data
	EE	0D	UA	11 = CR
	EF	0A	UA	12 = LF
	F0	19	UA	13 = End of Message
	F1	00	UA	14
	F2	00	UA	15
	F3	00	UA	Word 16
00	03F4	19		Permanent EOM

3.4.2.6 SECONDARY ADDRESS

The 4880 can be modified to use a secondary address by deleting the Parallel Poll enable function. During the modification the desired secondary address is stored in PROM and all of the changes shown in Table 3-6 must be made to fully enable the secondary address function.

TABLE 3-6 SECONDARY ADDRESS CHANGES

Prom	Address	PPE-Code	SA Code	Description
00	0104	02	10	Listen addressed flag bit
00	0124	04	20	Talk addressed flag bit
00	03AF	29	6F	Branch Address
00	03B0	03	02	Branch Address
00	0390	xx	Note 1	Secondary Address (Note 1)

NOTE

1. Secondary address character format = $0002^4\ 2^3\ 2^2\ 2^1\ 2^0$
   Address 14 decimal is stored as OE Hex

2. XX is a don't care code.

3.5 PWB CHANGES

3.5.1 Parallel Poll Enable

Parallel poll fast response is disabled in all standard units to make them compatible with the early Tektronix 4051 terminals. To enable the fast response logic, relocate the EOI jumper so it bridges F to E not + to E. This jumper is located on the top center of the main board.

4

Theory of Operation

4.1 BLOCK DIAGRAM DESCRIPTION

The 4880 Bus Interface Coupler block diagram is shown in Figure 4-1. The 4880 Interface is a microprocessor based device that transfers data in a bidirectional fashion between standard instruments and the IEEE 488 Instrument Bus. Each 4880 Interface contains the 488 Bus Drivers-Receivers, Program Memory, and the microprocessor. The Input and Output Logic sections are added as required to complete the particular 4880 Bus Interface configuration. Program changes are made to accommodate the different configurations.

The 488 Bus Driver-Receivers transfer data between the IEEE 488 Bus and the internal microprocessor. The microprocessor either acts on the input data or converts it into the output command word which is passed onto the instrument through the Output Logic. Instrument generated data is inputted through the Input Logic and outputted to the bus when the coupler is in the Talk mode.

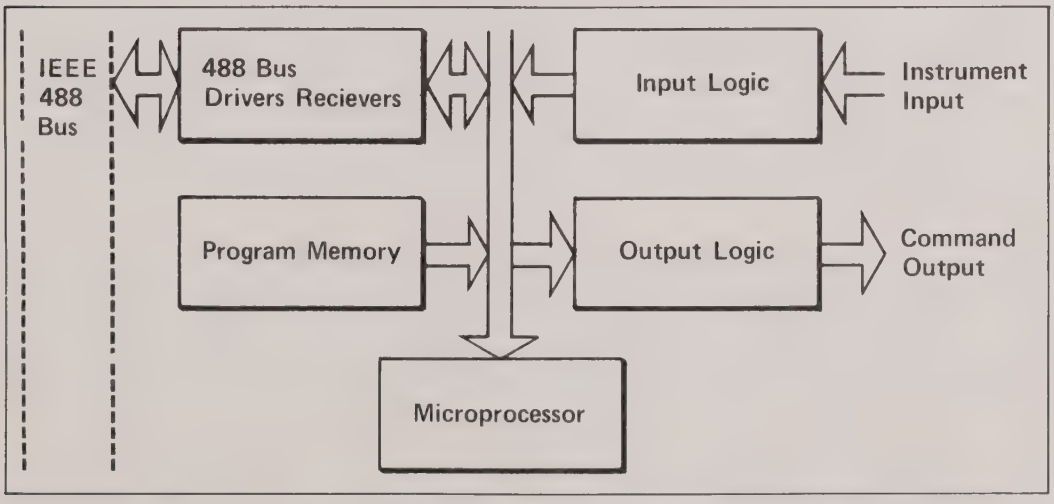


Figure 4-1 4880 Block Diagram

The 4880 Bus Interface operation is controlled by program commands stored in the PROM Memory. The microprocessor follows these commands to transfer data,

status and command functions between the 488 Bus and the instrument. Although the programs vary for the different 4880 configurations, all can be altered by the user to adapt the 4880 to his particular needs.

4.2 DETAILED LOGIC DESCRIPTION

4.2.1 Main Board (See Figure 7-1, sheets 1, 2, and 3)

The two phase microprocessor clocks are generated by U11, which performs a divide-by-eight operation on the clock pulses from the oscillator U6 and crystal Y1. Memory addressing is accomplished by an 12-bit memory address bus. The lower eight bits directly address the memory byte; the upper four bits operate a decoder, U4, which selects the device being addressed. Data is transferred to the microprocessor on a bidirectional bus. Data bus drivers U9 and U10 are used to drive the output latches in the Bus and Output Logic sections. Capacitor, C15 and resistor R9 are used to generate the power on clear pulse. Reset button, S2, shorts the capacitor to ground to generate a manual reset pulse. The IFC command coupled on capacitor C19 also generates a reset pulse.

Flip-Flop U40 senses the microprocessor's interrupt acknowledged status output on data line D0 during sync time. The Flip-Flop is then set for one clock time during which it forces all inputs off of the bidirectional data bus, thereby generating the RST7 command. The 8080 microprocessor program counter jumps to location 0038 hex as a result of this command. Depending upon the state of the jumper in pad I, interrupts come when the IEEE 488 ATN line goes low (I-A) or whenever the upper board has data ready (I-DR).

IEEE Bus Signals are terminated in resistor networks U24 and U32 before being gated onto the microprocessor data bus by gates U22, 23, 30, and 31. Bus output signals are stored in latches U25-28 before passing through the output drivers U33-36. Decoder U17 generates the latch load pulses and gate strobe pulses when the main decoder drops the AS7 line. Latch U18 is used to enable or disable the output drivers depending upon the state of the Bus EOI and ATN lines. Latch U18 can also be set under program control by raising data line D07 and generating strobe pulse 4 from decoder U17.

The 4884 power supply transformer can be switched to operate from 115 or 230Vac power by switch S4. Capacitor C1 filters the unregulated +22Vdc output. Regulator Q3 converts the unregulated voltage to +12 volts for the clock drivers. Regulator Q1 provides the +5Vdc for all the Couplers TTL logic chips. Capacitor C4 filters the unregulated -15Vdc output. Regulator Q2 converts the unregulated voltage to the -5Vdc microprocessor bias voltage.

4.2.2 I/O Card (See Figure 7-2, sheets 1 and 2)

Instrument data signals are transferred onto microprocessor data bus gates U1-U5 and U9-U13. Gate enabling strobes are generated by U19 which decodes the microprocessor generated address. The Flag Flip-Flop, U18, is set when the instruments data ready signal and EDR Flip-Flop, U18, are ANDED together in U25 to form a negative going 100 nsec wide set pulse. Connection of the data sources (typically an instrument) data ready signal either to J2 pin 6 or J2 pin 2 selects a

negative or positive going transition to generate the set pulse. Gate U26 inputs the instrument status line and polarity signal. Dual D flip flops, U27, output the 4880 generated trigger pulses to the instrument.

The instrument command output word is stored in latches U6-U8, U14-U16, and U21-U24. Data is loaded into these latches from the microprocessor data bus when the decoder U30 senses address line AS5 low and lower order address of 00 through 04. A lower order address of 05 enables gates U29 to input the instruments status onto the microprocessor data bus. Output transfer pulses and auxiliary command signals are generated under program control by loading data bits 0 through 3 into latch U32. The loading is accomplished by a clock pulse generated by lower order address 06 in conjunction with AS5 being low.

5

Maintenance

5.1 INTRODUCTION

This section describes the maintenance and troubleshooting procedures for the Model 4880 Bus Interface. The 4880 Bus Interface does not require periodic calibration and has no internal adjustments. This section also includes a brief description of the 4880s logic convention and symbols.

5.2 REFERENCE DESIGNATIONS

The 4880 Bus Interface is assembled in a one-half-rack-wide chassis with components mounted on circuit boards and the rear panel (see Figure 6-1). The circuit boards are mounted horizontally; the large bottom board is designated A1 and the top board is designated A2. Components on schematics and parts lists are designated by the partial reference designation; i.e., Q1 rather than the complete form, A1Q1. Board component locations are shown in Figures 6-2 and 6-3.

5.3 TROUBLESHOOTING PROCEDURES

This section describes procedures for locating operating and basic coupler problems. It is assumed that the user has a good grasp of his overall system, some basic electronic knowledge and has read the Couplers theory of operation in Section 4.1. Section 5.4 is a quick review of the more common digital logic symbols found on the Coupler schematics.

Basic troubleshooting involves following the Fault Isolation steps in Table 5-1 to narrow down the problem to a specific area. The majority of simple problems can be fixed by following the table and returning the faulty assembly to ICS Electronics. Consult the spare parts list or coupler parts list in Section 6.1 for correct part numbers and description when ordering any module, assembly or other replacement part.

Detailed troubleshooting of a microprocessor based system like the 4880 Coupler requires the use of a microprocessor analyzer[1] in addition to the standard oscilloscope and VOM. The oscilloscope and VOM are excellent for troubleshooting static circuit elements such as the power supply, oscillator-clock driver, frequency selector and the serial drives and logic. The oscilloscope can even be used to troubleshoot data words and bits if the oscilloscope is sync'd to the respective word clock or strobe pulse line. Data flow should be tracked forward to find the defective IC, using either the oscilloscope or microprocessor analyzer. Data addresses

are given in the schematics by combining the ASX line with the decoded strobe to produce an address according to the following formula:

address = 0 + ASX + 0 + strobe number

i.e., 4880 address switch is:

0 + AS7 + 0 + 6 from Figure 7-1 sheet 2
= 0 + 7 + 0 + 6
= 07 06 (hex)

Set the address into the microprocessor analyzer to observe the switch value being read by the microprocessor.

5.4 LOGIC CONVENTIONS

The unit uses positive logic, which means the normally active or high signal state which for LSTTL Logic is +3.5 ±1 volts and the inactive or low state is 0 ±0.5 volt. On the microprocessor data bus, the logic '1' level is +3.4 to +5Vdc. The high state is referred to as logic 1 and the low state is logic 0. The terms true and false relate to the signal being in or out of its active state and normally correspond to logic 1 and 0. However, for some compliment signals such as the input of a OR gate, the true or active state is the low signal level (0 volts).

Compliments of signals are indicated by an F or N suffix or by an inversion dot on the logic symbol. Complimented signals are always low when the original signal is high and vice versa. See Figure 5-1 for the standard logic symbols.

1-A microprocessor analyzer plugs into the microprocessor socket and lets the user observe the data flow to/from memory and I/O ports. A typical unit is the Model MPA-80/MPU-8080 manufactured by Current Electronic Design, Burbank, California, 213/841-0434.

WARNING

IF THE FAULT ISOLATION PROCEDURE REQUIRES INTERNAL MEASUREMENTS, ALWAYS REMOVE POWER WHEN DISASSEMBLING OR ASSEMBLING THE UNIT. USE EXTREME CAUTION DURING TROUBLESHOOTING, ADJUSTMENTS, OR REPAIR TO PREVENT SHORTING COMPONENTS AND FURTHER DAMAGE TO THE UNIT.

TABLE 5-1 MODEL 4880 FAULT ISOLATION STEPS

Symptom	Possible Fault	Check
No power or no POWER light	Blown fuse	Fuse on rear panel
	115/230V Switch	Switch on rear panel
	ac power	Power cord plugged into rear panel and ac outlet
	Broken LED	Check LED, CR8
	+5 volts shorted	+5v pins on J2 and J3
	Excessive ambient temperature +5 regulator in thermal shutdown	Check unit ambient and internal temperature
READY light off	Status lines open or wrong level	Input device not ready Input Status line open Output device not ready Output Status lines open
	Loose part after shipment	PROMs, microprocessor and cable connectors and any socket mounted part
	Microprocessor miss-start	Press RESET or turn POWER off for 10 seconds

TABLE 5-1 MODEL 4880 FAULT ISOLATION STEPS (continued)

Symptom	Possible Fault	Check
No TALKING or LISTENING light response	Wrong Address	Address switch setting Value in controller program Extended address only if PROM changed
	Reset not pressed after changing T, L or O switches	Press RESET
TALKING light on	T and O switches on	Address switch
	Untalk or listen address not sent	Controller program
	No data received	Input device
	Controller has not received data or a terminating character	Check input device: HP9825 needs a line feed. Tektronix 4051 needs a carriage return.
TALKING light off	L and O switches on	Address switch
	READY off	See READY above
	Wrong address	Address switch setting (3.1.2) Controller program
LISTENING light on	L and O switches on	Address switch
	Unlisten or talk address not sent	Controller program
LISTENING light off	T and O switches on	Address switch

TABLE 5-1 MODEL 4880 FAULT ISOLATION STEPS (continued)

Symptom	Possible Fault	Check
	READY off	See READY above
	Wrong address	Address switch setting (3.1.2)
		Controller program
No data transmission	Not in Talk Mode	See TALKING above
	External Data Ready inputs not connected properly	Check per 2.6
	Device not generating EDR signal	Device mode and operation
	Device trigger not present if required by external device	Controller program
No command output	Not in Listen mode	See LISTENING above
	Transfer pulse not sensed	Check connections per 2.7. Observe signals
	Transfer pulse not generated or data outputted	Check controller program for CR, LF, or commas
Device not following output commands	External device not in remote mode	Device controls or missing enable jumper in cable
	Cable error	See device instruction manual
		Check cable wiring
No SRQs	SRQ INHIBIT switch in	Release switch

TABLE 5-1 MODEL 4880 FAULT ISOLATION STEPS (continued)

Symptom	Possible Fault	Check
Unwanted SRQs	SRQ INHIBIT switch out	Depress switch
	Coupler not in talk mode	Controller program
No response to Parallel Poll	ATN not lowered after sending PPC Command and lowering E01	Controller program
	E - F jumper missing	See Section 3.5
	PPC, PPE commands missing	Controller program
	ATN off time not sufficient	Controller program
	ATN not turned on after or with E01	Controller program

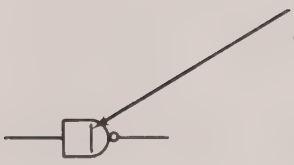
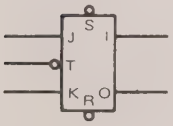
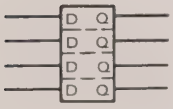
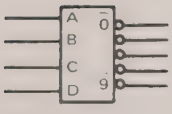
	Inversion dot	Part of a larger symbol. Indicates that the input or output signal is low when in the active or true state.
	Open collector bar	Bar on output indicates an open collector device without an internal signal pullup.
	NAND gate	Performs the NOT-AND function. Output is low when all inputs are high.
	NOR gate	Performs the NOT-OR function. Output is high when one or more inputs are low.
	Wired OR	Performs an OR function using only chassis wires. Output low when one or more inputs are low.
	Amplifier, (level shifter or inverter)	Performs signal current amplification or level shift function. Signal polarities shown by inversion dots.
	Inverter	Performs a logic signal inversion; always used with the inversion dot.
	Clocked Flip-Flop	Output changes state on negative edge of clock if J and/or K was true during clock time. Outputs set or reset if either Preset or Reset input grounded.
	Quad Latch	Four D or storage flip-flops in single package. Normally has both Q and $\overline{Q}$ outputs. Data loads while clock high, latched when low.
	Counter	Four cascaded flip-flops in a single package designed as a counter. Divides by 10, 12, or 16. Check an IC catalog for reset, clear and load signal definitiions.
	Decoder	Four line BCD to ten line decimal decoder. Outputs low when active.

Figure 5-1 Standard Logic Symbols

6

Parts List and Location

6.1 INTRODUCTION

This section contains all information necessary to locate, identify, and order parts. The listing of parts and information for an exact replacement are shown in the attached parts list. All components locations are identified by reference designators in the parts list and in the attached circuit board assembly drawings. Layouts for the units circuit boards are shown in Figures 6-2 thru 6-4.

6.2 REPLACEMENT PARTS

6.2.1 Standard Parts

All parts can be purchased directly from ICS Electronics Corporation, at current market price, plus a handling charge. However, since most parts are standard electronic components, it is suggested that they be secured locally for prompt replacement. The parts list gives all pertinent information including the recommended manufacturers. Where not noted, equivalent parts meeting the original part specifications may be substitued. A list of manufacturers by abbreviations is given in Table 6-1 and recommended spare parts in Table 6-2.

6.2.2 Special Parts

Parts marked with a Data Works, Fairchild Instrumentation, or an ICS part number should be procured directly from ICS Electronics Corporation. These parts are manufactured or selected to satisfy specific requirements. Substitution of other parts might not yield equivalent performance and will void any warranty.

6.2.3 Parts Ordering Information

All orders should be directed to ICS Electronics Corporation, at the address shown on the front page, or to ICS Electronics in care of your local representative. When ordering, be sure to include the following information:

a. Part description and reference designator
b. Part number, manufacturer, and stock number
c. Instrument model, serial number, and program revision level.

TABLE 6-1 List of Manufacturers by Abbreviations

Abbreviations	Company
ABC	Allen Bradley, Milwaukee, WI
ACT	Advanced Components Technology, Inc., Redwood City, CA
AEP	Alco Electronic Products, Inc., Lawrence, MA
AMA	Amaton, New Haven, CT
AMD	Advanced MicroDevices, Sunnyvale, CA
AMP	Amp Incorporated, Harrisburg, PA
ANS	Ansley Electronics Corp., Los Angeles, CA
APH	Amphenol Corp., Oakbrook, IL
ARC	Arco, Commack, NY
ARI	Aries Industries, Inc., Gardena, CA
AUG	Augat Inc., Attleboro, MA
BEC	Beckman, Heliport Division, Fullerton, CA
BEL	Belden Corp., Richmond, VA
BOR	Bourns, Riverside, CA
BUD	Budwig, Los Angeles, CA
BUS	Bussmann, Earth City, MO
CAC	Circuit Assembly Corporation, Costa Mesa, CA
CAN	Cannon, Santa Ana, CA
CEL	Cellotape, Sunnyvale, CA
CHY	Cherry Electrical Products Corp., Highland Park, IL
CJO	Cinch Manufacturing Co., Elk Grove Village, IL
CMS	Component Manufacturing Service, Bridgewater, MA
CDE	Cornell Dublier, Newark, NJ
CNT	Centralab, Los Angeles, CA
COR	Corcom Inc., Chicago, IL
CRN	Corning Glass Works, Corning, NY
CTS	CTS Corporation, Elkhart, IN
DAL	Dale Electronics Incorporation, Columbus, NB
DIA	Dialco, Brooklyn, NY
DWI	Data Works Instrumentation, (See ICS)
EPI	Epitek, Kanata, Ontario, Canada
ERI	Erie Technological Products, Erie, PA
EXL	Excel, Chicago, IL
FCL	Freedom Crystal Lab, Freedom, CA
FIS	Fairchild Inst. & Controls Div., (See ICS)
FLK	Fluke, Santa Clara, CA
FSC	Fairchild Semiconductor Div., Mountain View, CA
GHI	Grayhill, La Grange, IL
GOR	Gordos Corporation, Bloomfield, NJ

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TABLE 6-1 List of Manufacturers by Abbreviations - Continued

Abbreviations	Company
HEY	Heyboer, Grand Haven, MI
HHS	Herman H. Smith, Inc., Brooklyn, NY
HP	Hewlett-Packard
ICS	ICS Electronics Corporation, San Jose, CA
IER	International Electronics Research Corporation, Burbank, CA
INL	Intel, Sunnyvale, CA
IRC	TRW/IRC Resistors, Philadelphia, PA
ITT	ITT General Controls, Glendale, CA
JAR	Jarome Wire, Mountain View, CA
KEM	Kemet, Greenville, SC
KOS	Koszeigi, South Bend, IN
LFS	Little Fuse Inc., Des Plaines, IL
LOP	Zollin J. Lopaugh, San Francisco, CA
LYN	Lyntron, Inc., Burbank, CA
MED	Meadows Manufacturing, Sunnyvale, CA
MIN	Minicomputer Accessories, Sunnyvale, CA
MLX	Molex Products Co., Downers Grove, IL
MON	Monsanto, Palo Alto, CA
MOT	Motorola Semiconductor Products, Inc., Phoenix, AZ
MPI	Micro Plastics Inc., Chatsworth, CA
MSC	Master Specialities Co., Costa Mesa, CA
NAT	National Semiconductor Ltd., Plattsburgh, NY
NIC	Nichicon, Chicago, IL
PAN	Panduit, Tinley Park, IL
PCL	Precision Crystal Lab, Santa Monica, CA
PNS	Panasonic, Secaucus, NJ
RAY	Raytheon, Mountain View, CA
RCH	Richlock, Chicago, IL
RGA	RG Allen, Van Nuys, CA
SAE	Stanford Applied Engineering, Long Beach, CA
SCN	Scanbe, El Monte, CA
SEK	Seiko Circuits, Sunnyvale, CA

TABLE 6-1 List of Manufacturers by Abbreviations (Continued)

Abbreviations	Company
SHO	Shoin, Japan
SIG	Signetics Corp., Sunnyvale, CA
SMN	Siemens, Iselin, NJ
SPC	Spectra Strip
SPR	Sprague Electronics, Chicago, IL
SWC	Switchcraft, Inc., Chicago, IL
TEK	Tektronics, Inc., Beaverton, OR
TEM	Temple Industries, Inc., Tecate, CA
TEX	Textool, Irving, TX
THC	Thermalloy Co., Dallas, TX
TI	Texas Instruments, Semiconductor Div., Dallas, TX
UCC	United Chem-Com, Rosemont, IL
USE	USECO, Van Nuys, CA
VIK	Viking, Chatsworth, CA
WDC	Western Digital Corp., Newport Beach, CA
WFD	Wakefield Engineering, Inc., Wakefield, MA
WIN	Winchester, Oakville, CT

6.3 PARTS LIST

The parts list (Table 6-3) contains all components and sub-assemblies that make up the unit. Subsequent Tables 6-4 and 6-5 break the main board assembly (A1) down to the component level. Table 6-6 breaks the I/O Board Assembly (A2) down to the component level.

The parts list tables contain both the ICS Electronics Corporation stock numbers and the manufacturers' true part numbers where applicable. True manufacturers' part numbers are not shown for industry standard parts nor items unique to the 4880 Coupler.

TABLE 6-2 4880 RECOMMENDED SPARE PARTS LIST

For assembly level sparing order the following: Item 1 or 2, Item 3, and Item 4A or 4B.

For component level sparing, items 5 through 34 may be ordered separately or together in kit form as 4880 Spare Parts Kit, P/N 111263, (see item 34). Refer to Stock Number when ordering from ICS Electronics.

Item	Qty.	Mfgr.	Part Number	Description	Stock No.
1	1	ICS	111002	Assy. Main Board	111002
2	1	ICS	111019	Assy. Main Board Less Rear Panel	111019
3	1	ICS	111006	Assy., I/O Card	111006
4A	5	LFS	313001	Fuse 3AG 1 Amp	900002
4B	5	LFS	313000.5	Fuse 3AG 1/2 Amp	900001
5	1	ICS	10079	Transformer	125000
6	1	GHI	76B08	Switch, Rocker 8 Posn.	907011
7	1	ICS	125005	Switch 3 Posn.	125005
8	1	FSC	UA7805	Regulator +5V	730340
9	1	FSC	UA7905	Regulator -5V	737905
10	1	FSC	UA7812	Regulator +12V	737812
11	2		IN4001	Diode, 50V, 1A	714001
12	2	MOT	MR 502	Diode, 200V, 3A	710502
13	2	FSC	FLV160	LED, RED	710160
14	1	ICS	904001	Crystal 14.745 MHz	904001
15	1	AMD	8080A	Microprocessor	798080
16	1	ICS	2708	PROM, with 4880 Program	792708
17	1	AMD	74LS138	IC, DCDR	742138
18	1		74LS13	IC,Schmitt Trig.	742013
19	1		74LS04	IC, Hex Inv.	742004
20	1	AMD	2112A-04	RAM 4 x 256	792112
21	1	SIG	8T97	IC, DVR	738097
22	1		74LS197	IC ÷16	742197
23	1		74LS00	IC, QUAD NAND	742000
24	2		74LS03	IC, QUAD NAND	742003
25	1		74LS74	IC, D F/F	742074

*See ICS's latest 4880 Recommended Spare Parts list for current prices.

TABLE 6-2 4880 RECOMMENDED SPARE PARTS LIST
(Continued)

Item	Qty.	Mfgr.	Part Number	Description	Stock No.
26	1		74LS10	IC, 3 INput NAND	742010
27	1		7406	IC, Hex DVR	740006
28	2		74LS75	IC, QUAD Latch	742075
29	1		7438	IC, DVR	740038
30	1		74107	IC, JK F/F	742107
31	1	ABC	316E302622	RES. NET 3K/6.2K	697002
32	1	DAL	898-1-R3.3K	RES. NET 3.3K	697001
33	1		2N3906	Transistor, PNP	723906
34	1	ICS	-	4880 Spare Parts Kit (includes items 4A, 4B)	111263

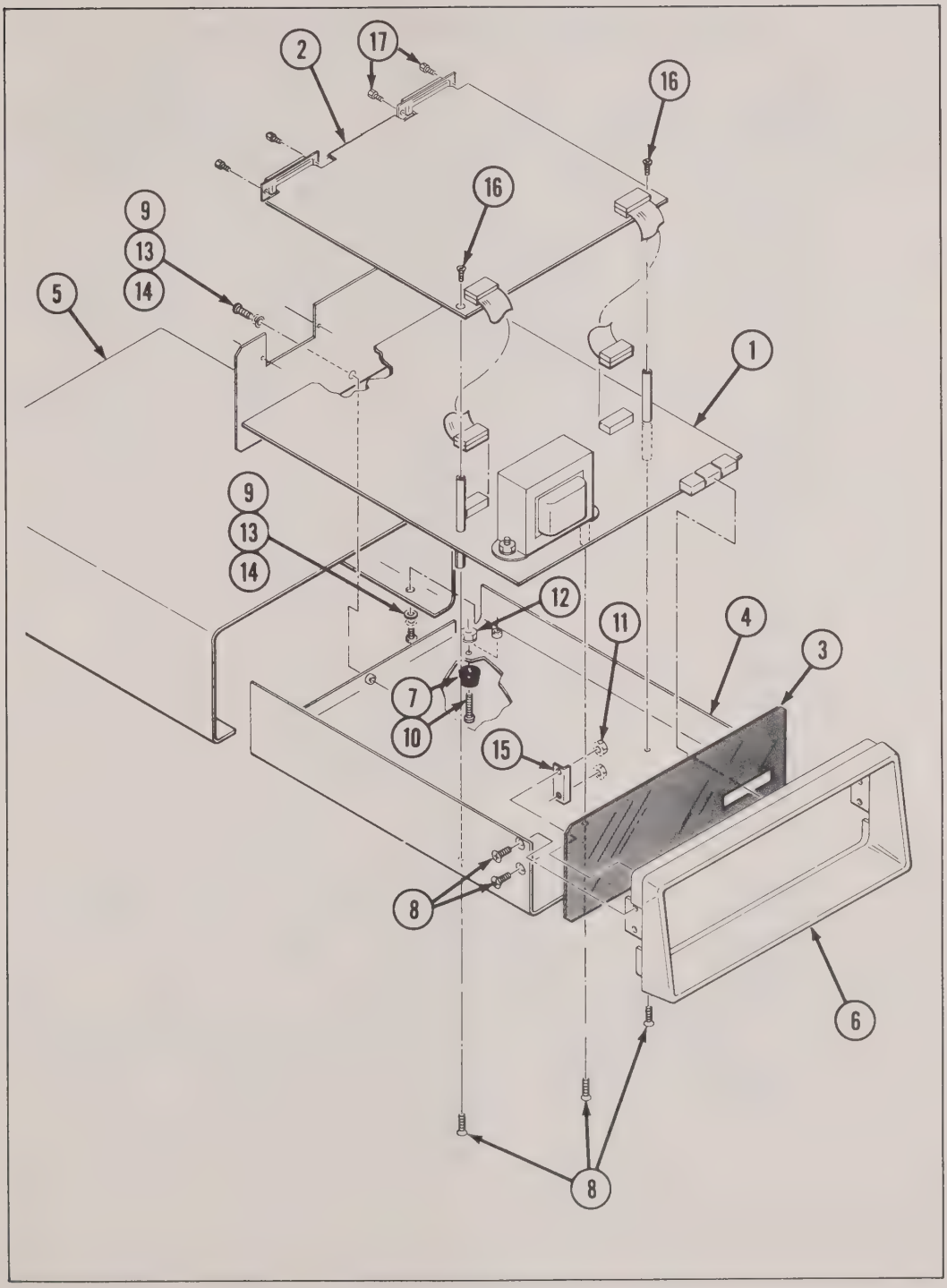


Figure 6-1 4880 Coupler Exploded Assembly

TABLE 6-3 4880 IEEE COUPLER - PARTS LIST

Identification No.	Stock Number	Qty. Per Assem.	Description	Ref.	Mfgr.	Mfgr.P/N
1	111002	01	ASSY MAIN BOARD	A1		
2	111019	01	ASSY, 4880 I/O BOARD	A2		
3	112033	01	FRONT PANEL			
4	112237	01	BASE PLATE			
5	112238	01	COVER			
6	112239	01	BEZEL			
7	908000	04	FOOT, MTG			
8	412606	08	SCREW, #6-32 x 3/8 FH			
9	410806	05	SCREW, #8-32 x 3/8 PH			
10	410408	04	SCREW, #4-40 x 1/2 PH			
11	422600	04	KEPNUT, #6			
12	422400	04	KEPNUT, #4			
13	431800	05	WASHER, SPLIT-LOCK, #8			
14	430800	05	WASHER, FLAT, #8			
15	112258	02	CLIP, RETAINING			
16	410606	02	SCREW, 6 X 32 X 3/8, PH			
17	490005	02	STUD, FEMALE LOCKING	(J2)	CJO	BD-20418-2
18	112096	01	ASSY, MEMORY EXP. MODULE	A3		
19	112001	01	LABEL			

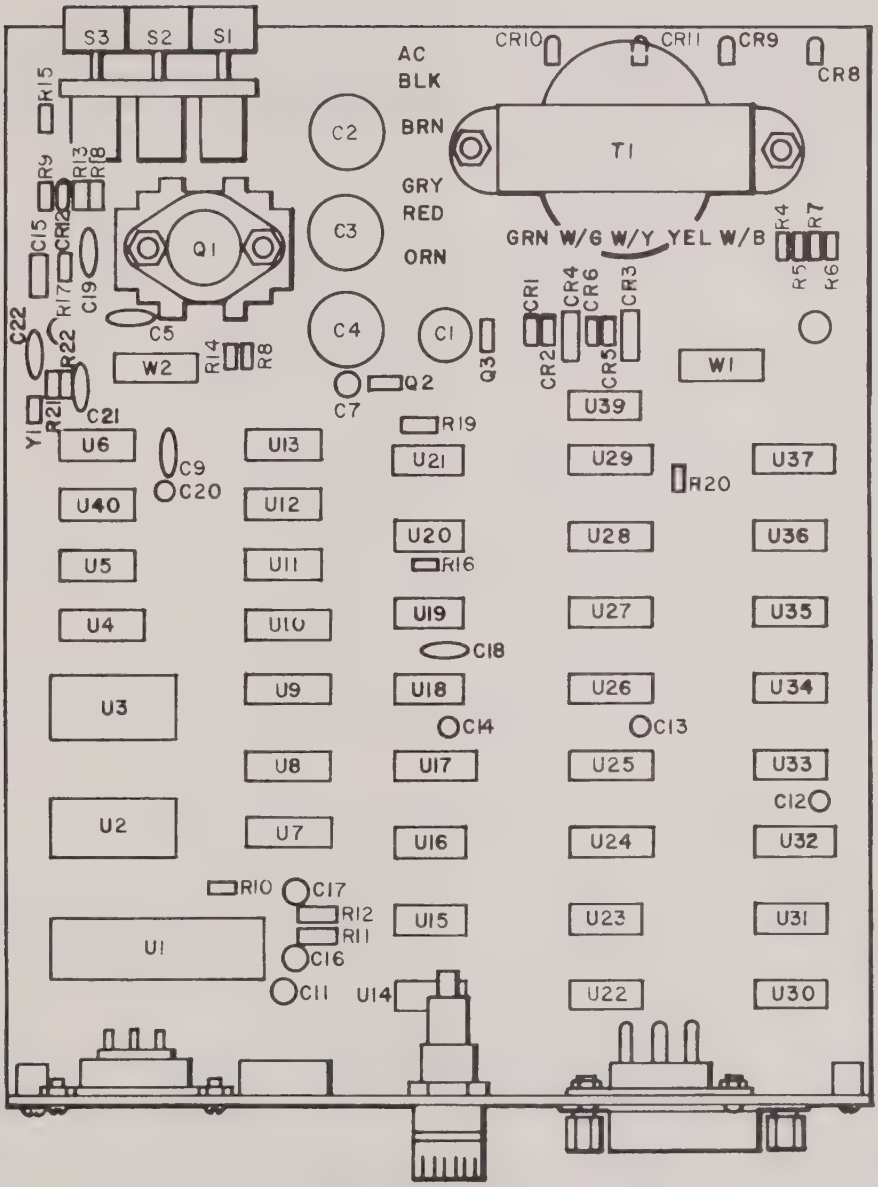


Figure 6-2 Assembly 4880 Main Board

TABLE 6-4 4880 MAIN BOARD PARTS LIST

Stock Number	Qty. Per Assem.	Description	Reference	Mfgr.	Mfgr.P/N
907012	01	SWITCH, SLIDE 115/230VAC	S4		
902009	01	RECEPTABLE, AC, POWER	J4		
112257	01	CABLE, HARNESS			
410408	04	SCREW 4-40 x 1/2 PH, PHL	(S4), (J4)		
421400	04	NUT #4 SMALL PATTERN	(S4), (J4)		
431400	04	LOCKWASHER #4	(S4), (J4)		
111011	01	REAR PANEL			
112256	01	4880 ASSY-PCB			
900002	01	FUSE, 3AG, 1 AMP	F1	LFS	313001
901001	01	FUSEHOLDER, 3AG	XF1	LFS	342004
490001	02	MTG STUD, STANDOFF, (M)	(J1)	ICS	0380-0643

TABLE 6-5 PC BOARD ASSEMBLY PARTS LIST

Stock Number	Qty. Per Assem.	Description	Reference	Mfgr.	Mfgr.P/N
111004	01	P.C. BOARD			
110079	01	TRANSFORMER, 10079	T1		
125005	01	SWITCH ASSY, 3 POSN	S1-3		
907011	01	SWITCH, ROCKER, 8 POSN	S5	GHI	76B08
903005	01	SOCKET, 16 PIN, RT ANGLE	(S5)	AUG	516-AG7D
902004	01	CONNECTOR, 24 PIN	J1	APH	57-20240-2
906001	01	HEATSINK	(Q1)	IER	LAT03B5CB
730340	01	REG., UA7805, POS, +5V	Q1		
737905	01	REG., UA7905, NEG, -5V	Q2		
737812	01	REG., UA7812, POS, +12V	Q3		

TABLE 6-5 PC BOARD ASSEMBLY PARTS LIST
(Continued)

Stock Number	Qty. Per Assem.	Description	Reference	Mfgr.	Mfgr.P/N
714001	05	DIODE, IN4001, 50V, 1A	CR1,2,5,6		
710502	02	RCTFR, MR502, 200V,3A	CR3,4	MOT	
710160	04	LED, RED	CR8-11	FSC	FLV160
904001	01	CRYSTAL, 14.745 MHz, PC 18	Y1		
514207	01	CAP, ELEC, 200UF, 35V	C1	TEM	411-200-35
562152	03	CAP, ELEC, 1500UF, 15V	C2-4	TEM	411-1500-15
535104	03	CAP, CERAMIC, 0.1UF, 50V	C5,9,10	ERI	8121-050-L51-104M
521475	05	CAP, TANT, 4.7UF, 10V	C7, 11-14	ITT	TAG F20-4.7-10/50
511276	01	CAP, TANT, 27 UF, 35V	C15		CSR13 C276KL
522106	02	CAP, TANT, 10UF, 16V	C16,17	ITT	TAG F20-10-16
539102	01	CAP, DISK, .001 UF	C18	ERI	831-000-YSFO-102X
533103	01	CAP, DISK, .01 UF	C19	ERI	5835-000-Y5U0-103E
548240	02	CAP., 24 PF, 500V	C21, C22		
602222	03	RES, 2.2K, 1/4W 5%	R21-22,16		RC07GF222J
602161	05	RES, 160 , 1/4W 5%	R4-7,17		RC07GF161J
602333	06	RES, 33K, 1/4W 5%	R8,9,10,14 15,19		RC07GF333J
603331	02	RES, 330 , 1/2W 5%	R11,12		RC07GF104J
602104	02	RES, 100K, 1/4W 5%	R13		RC07GF104J
602224	01	RES, 220K, 1/4W 5%	R18		RC07GF224J

TABLE 6-5 PC BOARD ASSEMBLY PARTS LIST
(Continued)

Stock Number	Qty. Per Assem.	Description	Reference	Mfgr.	Mfgr.P/N
602103	01	RES, 10K, 1/4W 5%	R20		RC07GF103J
798080	01	9080A/P8080A	U1	AMD	
792708	01	2708	U2	ICS	
742138	02	74LS138	U4, U17	AMD	
742013	01	74LS13N	U5		
742004	02	74LS04N	U6, U16		
738097	02	8T97	U9, U10	SIG	
742197	01	74LS197N/9LS197N	U11		
742002	02	74LS02N/9LS02	U13, U19		
742003	06	74LS03N/9LS03N	U14-15, U22-23, U30-31		
741074	01	74S74N/9S74N	U18		
742010	02	74LS10N/9LS10N	U20, U12		
740006	01	7406N	U21		
697002	02	RES, NET, 3.3K, 6.2K	U24, U32	ABC	316E302622
742075	05	74LS75N/9LS75N	U25-29		
740038	05	7438N	U33-36, U39		
697001	01	RES, NET, 3.3K	U37	DAL	898-1-R3.3K
742107	01	74LS107N/9LS107N	U40		
441614	04	SPACER, MALE-FEMALE	(T1)		
422600	04	KEPNUT #6	(T1) (Q1)		
430800	04	WASHER, FLT. #8	(T1) (Q1)		
411608	04	SCREW, 6 X 32 X 1/2, PH,PHL			
903006	04	SOCKET, 16 PIN	(U7, 8) (W1, 2)		
903007	02	SOCKET, 24 PIN	(U2, 3)		
903008	01	SOCKET, 40 PIN	(U1)		
442624	02	STANDOFF, SWG, 1-1/2 X 6-32	NONE	LYN	L6910-24-3C
490003	02	CHASSIS, FASTENERS	NONE	USE	1590C11

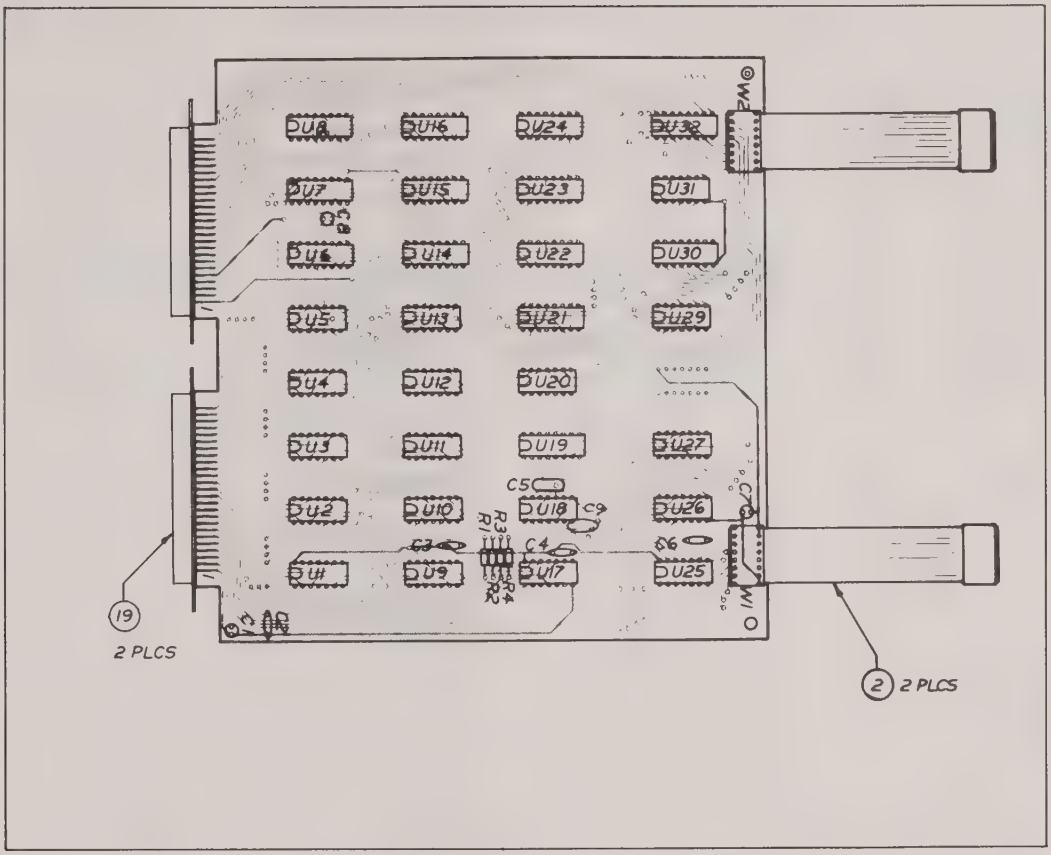


Figure 6-3 Assembly 4880 I/O Card

TABLE 6-6 4880 I/O BOARD PARTS LIST

Stock Number	Qty. Per Assem.	Description	Reference	Mfgr.	Mfgr.P/N
111008	01	P.C. BOARD, 11008		ICS	
740006	01	HEX DVR OC SN7406N	U17	TI	7406N
742074	01	DUAL D F/F SN74LS74N	U27	TI	74LS74N
742138	03	IC DCDR 74LS138	U19,29,30	TI	74LS138N
742000	02	QUAD NAND SN74LS00N	U18,25	TI	74LS00N
742004	02	IC, HEX INV SN74LS04N	U20,31	TI	74LS04N
742075	11	QUAD LATCH SN74LS75N	U6-8,14-16 21-24,32	TI	74LS75N
742003	12	QUAD NAND OC SN74LS03N	U1-5,9-13, 26,29	TI	74LS03N
602103	04	RES, 10K, 1/4W 5%	R1-4	ABC	RC07GF 103J
521475	03	CAP, TANT, 4.7 uf, 10V	C1,7,8	ITT	TAG20F 4.7/10
548101	04	CAP MICA 100 pf	C5	ARC	CM0SFD 101J03
533103	01	CAP DISC .01 uf	C2-4,6		
539102	02	CAP DISC .001 uf	C9		
902003	02	CONNECTOR 50-PIN-		APH	57-30500
112095		CABLE, 16 CONDUCTOR	W1,2		

7

Drawings, Diagrams, Wire Lists

This section includes the following figures:

7-1 Model 4880 Main Board Logic Diagram
7-2 Model 4880 I/O Card Logic Diagram

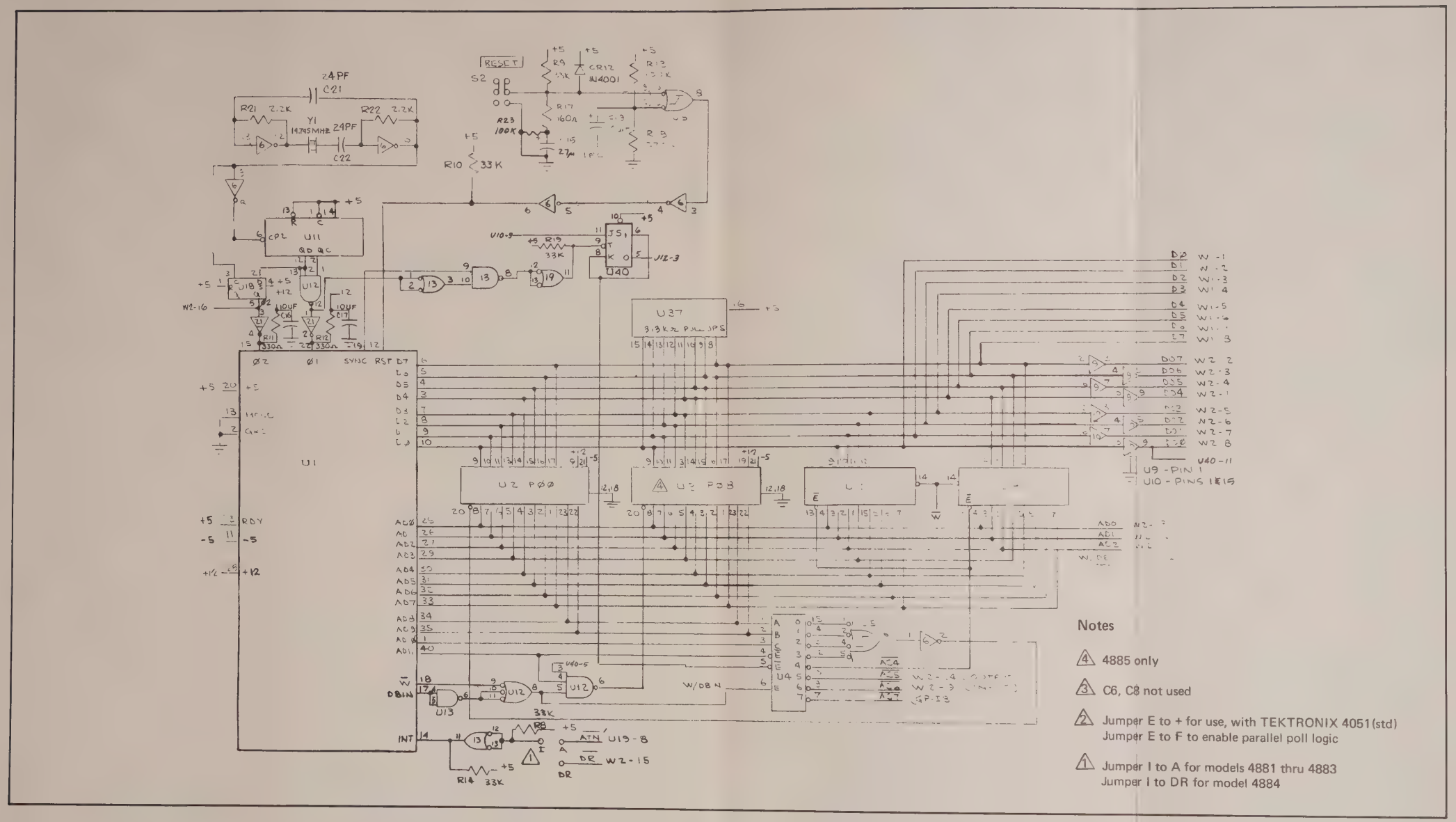


Figure 7-1 Model 4880 Main Board Logic Diagram

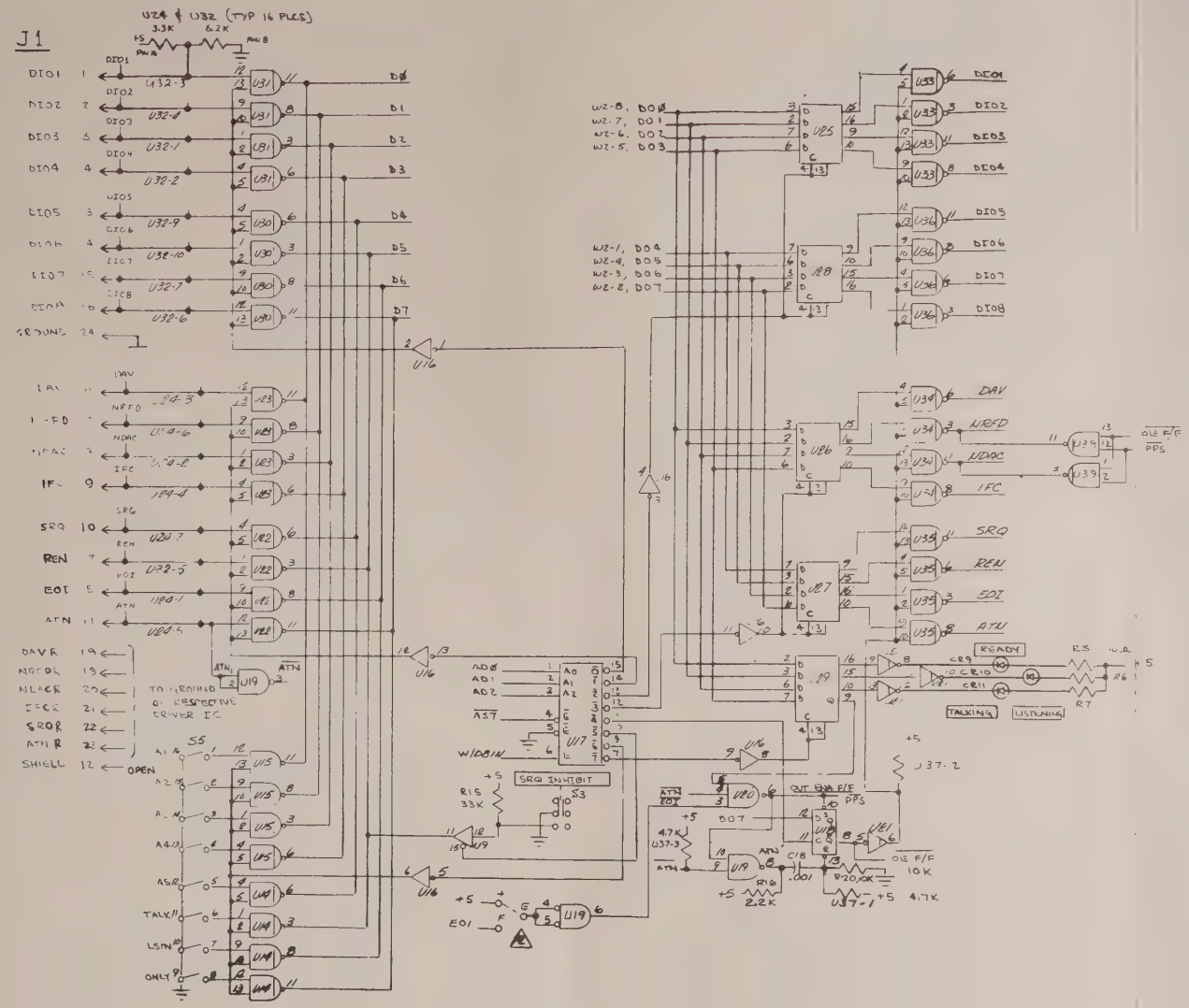


Figure 7-1 Model 4880 Main Board Logic Diagram (Continued)

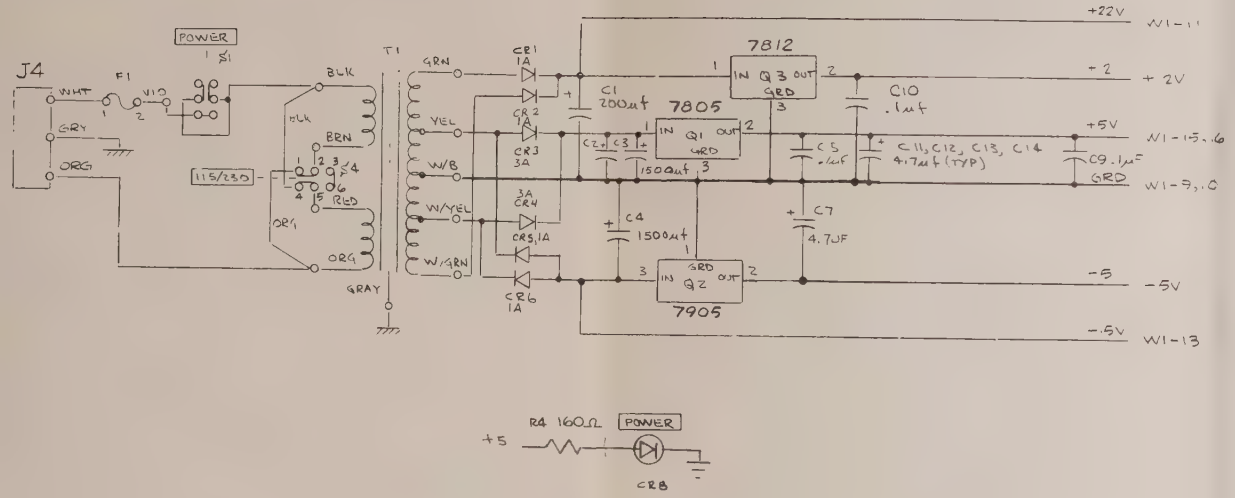


Figure 7-1 Model 4880 Main Board Logic Diagram (Continued)

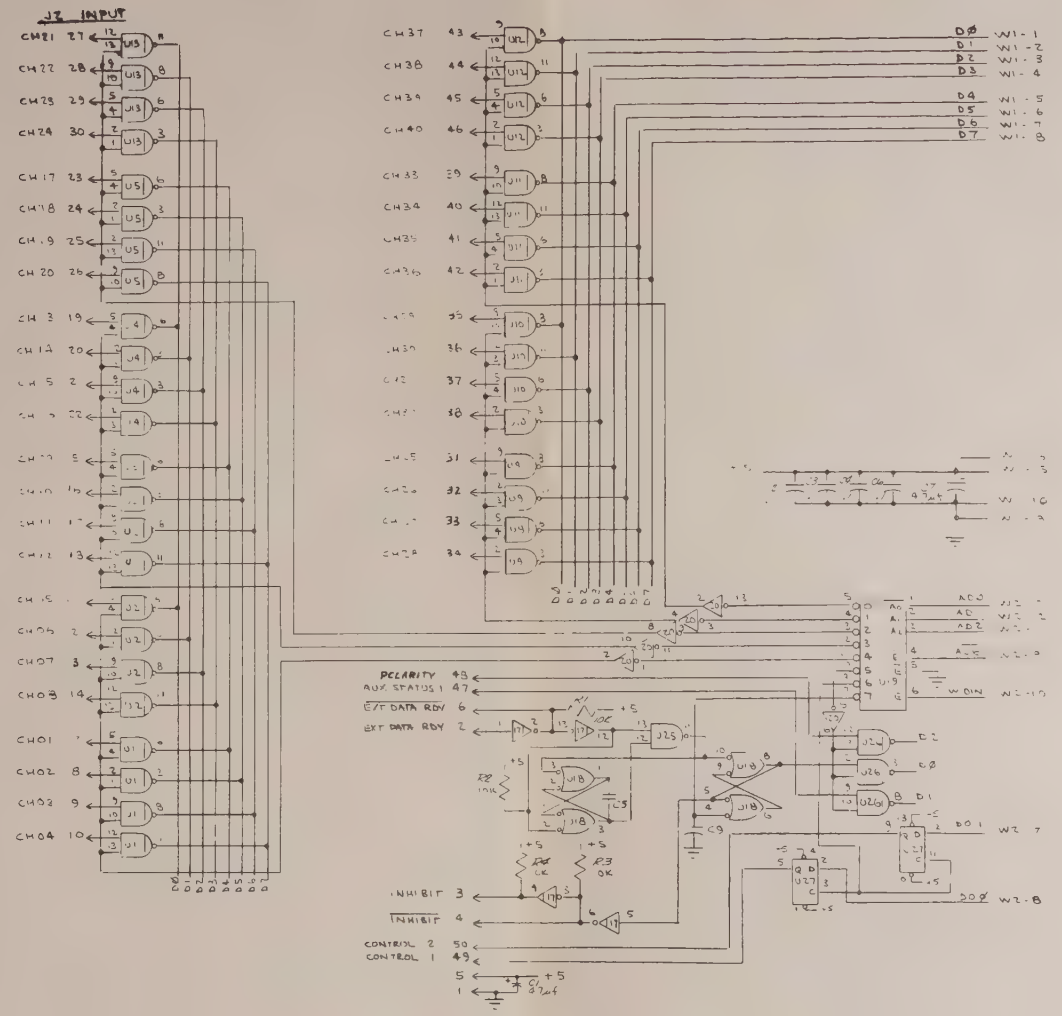


Figure 7-2 Model 4880 I/O Card Logic Diagram

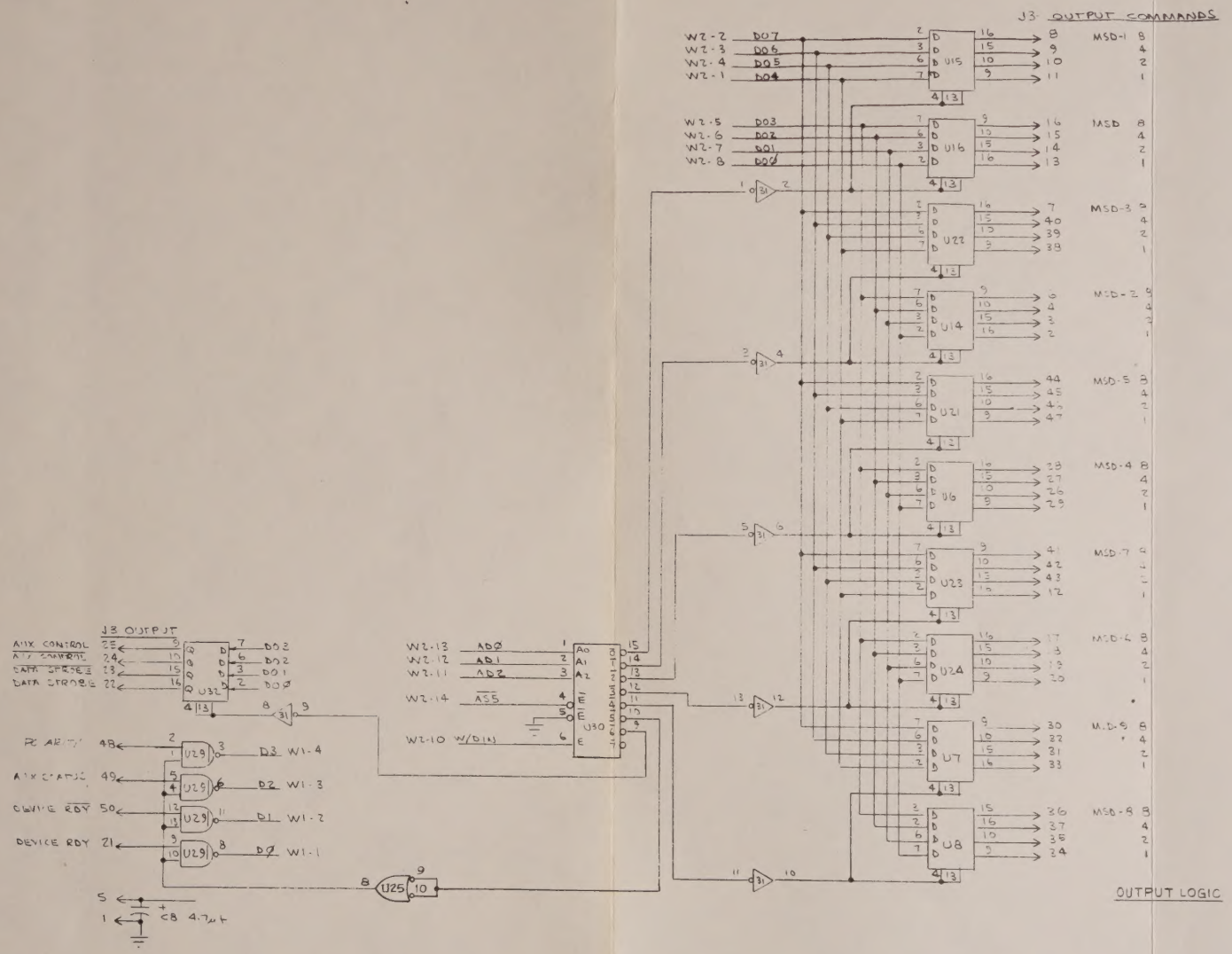


Figure 7-2 Model 4880 I/O Card Logic Diagram (Continued)

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